1-MHZ LINE DETECTOR FOR INTRA-BUNCH-TRAIN MULTICHANNEL FEEDBACK*

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Abstract

The measurement and control of the electron bunch length is one of the key diagnostics in linac-based free-electron lasers to reach the required peak current in the electron bunches. In order to use the multi-channel signals from longitudinal bunch shape measurements for intra train feedback for the European XFEL, line readout rates in the MHz range and low latencies are required, which is far more than commercial multichannel radiation detectors (line cameras) can provide. The paper presents a 256 channel detector that allows analyzing optical or infrared radiation with 1 MHz repetition rate and a few microseconds latency using photodiode arrays, as needed for synchrotron radiation monitors, electro-optical bunch length measurements, or other laser based diagnostics. The proposed architecture aims at high frequency readout with low latency by using a multichannel electronic front-end designed for HEP, combined with Si or InGaAs detector arrays with very fast response time, and a low-latency data acquisition system. Currently, the device is at the conceptual design stage.

INTRODUCTION

FLASH and the European XFEL (E-XFEL) are linac-based free electron lasers which operate in pulsed mode with repetition rate of 10 Hz and a minimum bunch-to-bunch spacing of 1 µs and 220 ns, respectively [1], see Figure 1. The 1 MHz line rate of the proposed detector will be also sufficient for the E-XFEL due the latency of the feedback loop of a few microseconds. It may be used in this case to measure e.g. every fifth bunch in a train.

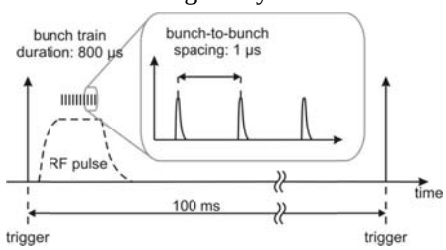

Figure 1: Pulse mode timing scheme for FLASH operation. The minimal interval between bunches in a train (1 µs) constitutes the most important timing constraints for the proposed detector.

In order to operate the electron accelerators with stability needed to efficiently produce FEL light, the accelerating parameters have to be kept in a tight range by feedback loops acting on phase and amplitude of the accelerating structures with a few microsecond latency. Some of the devices which could act as sensors for this feedback loops are based on line detectors like the electro-optical bunch length monitor or the synchrotron light monitor to detect energy and energy spread.

Since commercially available line detectors do not fulfil the requirements in terms of line rate, low latency, and integration into the feedback system [2], it is planned to develop a flexible detector system which supports a 1 MHz line rate and can be equipped with different types of line arrays.

In the following the currently envisaged applications of the detector are briefly described accompanied by a description of the proposed detector architecture with special attention paid to semiconductor sensors and electronic front-end. At present, the detector is in the design phase.

Applications

The spectrally encoded electro-optical bunch length monitor [3] is based on a pulsed ytterbium fiber laser probing the field-induced birefringence in an electro-optically active crystal (GaP) with a laser pulse at 1030 nm (in the near-infrared). The time structure of the chirped laser pulse is modulated with the Coulomb field (THz-radiation) of the electron beam. The known wavelength to time mapping of the chirped laser pulse allows to decode the time profile of the laser pulse, and therefore the longitudinal bunch profile, with an accuracy as good as 200 fs from the single shot spectrum of the laser pulse.

The synchrotron radiation monitor (SRM) [4][5] records online the transverse beam profile of the electron bunches in the third dipole of the first bunch compressor at FLASH by imaging the visible part of the emitted synchrotron radiation onto a CCD camera. The horizontal beam position and horizontal profile are completely governed by the beam energy and beam energy spread due to the relatively large dispersion of the bunch compressor of 300 mm to 390 mm for deflecting angles of 16° to 20°. The resulting energy resolution of the SRM is about $1 \cdot 10^{-4}$. The CCD camera is equipped with an image intensifier which can be used as a fast gate. By adjusting the gate and delay of the camera timing, single bunches can be recorded out of a bunch train, however, the readout of the CCD is too slow to resolve more than one electron bunch within a bunch train.

Other possible applications for FLASH and the European XFEL are ultra-fast laser diagnostics of the injector-, the seed-, or the pump-probe-lasers, other laser-based diagnostics, and equipped with different sensors, for single shot X-ray detection.

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DETECTOR ARCHITECTURE

This section presents the proposed detector architecture. Selected aspects of the detector building blocks are presented in detail.

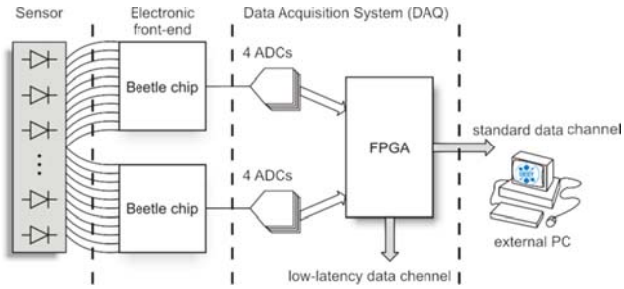

Figure 2: Proposed detector architecture.

Figure 2 presents the block diagram of the proposed detector architecture which can be divided into three major functional blocks:

- sensor – a Photodiode Array (PDA) with 256 independent channels
- electronic analogue front-end – a multichannel Integrated Circuits (ICs) originally developed for a High Energy Physics (HEP) experiments
- Data Acquisition System (DAQ) – a block based on Field-Programmable Gate Array (FPGA) responsible for data digitization and processing.

The energy of incident light of appropriate wavelength is collected by a PDA and then translated into an electrical form. Due to its low magnitude and short duration, the electrical signal needs to be conditioned with specialized electronic front-end in order to facilitate digitization and further data processing within DAQ.

Semiconductor Detector

The presented two major application of the detector require sensing radiation from two separated wavelength bands. As a consequence two different semiconductor detectors are taken into account:

- InGaAs – 900 nm to 1700 nm, for infrared (IR) radiation in EO bunch length measurements
- Si – 350 nm to 1000 nm, for visible synchrotron radiation detection and laser diagnostics

The detector is constituted by an array of photodiodes with common cathodes and individual anodes that work in photoconductive mode – i.e. the diodes are reversely biased all the time.

There are several parameters that need to be taken into account while selecting the most appropriate PDAs.

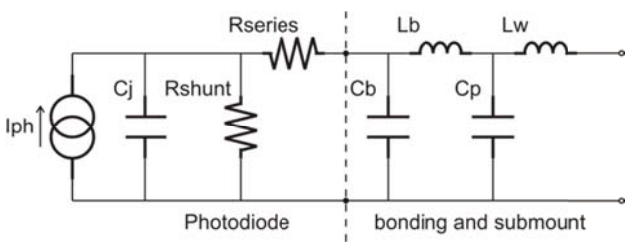

Figure 3: Equivalent circuit of a photodiode based on [6].

Usually a mounted (packed) diode is modelled using equivalent circuit shown in Figure 3, where:

- Iph represents photocurrent caused by incident light of appropriate wavelength
- Cj is a diode junction capacitance which is heavily dependent on reverse bias voltage and typically does not exceed several pF
- Shunt resistor (Rshunt) models dark current of the photodiode and often can be neglected due to its high value in order of magnitude of hundreds of mega ohms
- Series resistance (Rs) is typically in range of few tens of ohms.
- Cb is a capacitance of the photodiode's bonpad
- Cp embodies the stray capacitance of the package which in this case is ceramic epoxy with thin film metallization
- Lb and Lw represent inductance introduced by wire bonding and wires on the ceramic epoxy (the photodiode's carrier), respectively

Electro-optic characteristics of a photodiode are usually depicted using quantum efficiency (or spectral responsivity) as a function of incident light wavelength at given temperature. A sensor capacitance (Cj) characteristic as a function of reverse bias voltage is another important figure of merit.

Apart from electric and electro-optic features of the PDA, we need to take into account the optic apparatus used in the experiments.

Electronic Analogue Front-End

Electronic front-end is constituted by two Beetle chips which are multichannel readout ICs designed for HEP experiments at CERN. It was designed to comply with 40 MHz bunch crossing repetition.

However due to its primary application the Beetle chip introduces extra latency due to analogue pipeline [7]. The electrical signal which comes from the sensor is being conditioned (amplified, shaped) before being sampled and stored with a set of analogue memory cells. The data from the pipeline are read out upon an external stimulus (trigger). The minimal pipeline depth is 10 stages. Taking into account additional time for data to be valid at all output ports and some header bits, the latency of the analogue front-end is expected to be not lower than around 1.3 μs.

Another important aspect of the detector is electronic noise introduced by the analogue front-end which is described by Equivalent Noise Charge (ENC). This figure of merit is heavily dependent on the capacitance that the IC sees at its input. Some calculations have been done in order to estimate expected signal-to-noise ratio and number of bits for the ADCs. The ENC for the Beetle chip is given by [7]:

$$\mathrm{ENC} = 547\,\mathrm{e}^- + 52.64\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{Cin},$$

where Cin is the capacitance "seen" by the Beetle's analogue inputs (sum of stray and junction capacitances). Assuming the Cin to be equal 20 pF and electric input

signal value of $Qs = 100\,ke^-$, we can estimate the Signal-to-Noise Ratio $SNR = Qs/ENC = 36\,dB$.

Digital Back-End

The electrical signals from the Beetle chip are fed into the data acquisition (DAQ) module equipped with eight independent 14-bit analogue-to-digital converters. The chosen digitizer card (TAMC900 from TEWS [8]) provides the sampling speed of up to 105 MSps, which is more than twice the minimum required value.

The detector can operate in two modes: real-time (using low-latency channel) and off-line diagnostics (using standard channel). In the latter mode, the DAQ module is responsible for archiving the complete data from the sensor. Such an approach provides means for the off-line data analysis, but it is not really usable for real-time feedback systems.

In the real-time mode, the signals from the sensor are processed using the algorithms implemented in the on-board FPGA device. Only a few key parameters characterizing the most important signal distribution features (e.g. peak value, centre of mass, and asymmetry) will be compute. The digitizer board contains an FPGA from the Xilinx Virtex-5 family, which is equipped with specialized DSP slices. On-board pre-processing reduces the amount of data to be transmitted. The fast digital processing combined with a low-latency high-speed serial link enables the module to become a part of the real-time LLRF control loop [9].

Hardware Layout

Thee detector will be realized as two modules – a sensor and digitizer (DAQ) boards. The sensor board will comprise the PDA and the analogue front-end (Beetle chips) together with some auxiliary electronics. The digitizer board will be equipped with an FPGA device and serial data link for communication with the control system. Since the detector is planned to be integrated into the µTCA architecture, it was decided to use the TAMC900 ADC from TEWS which has proven to be very reliable.

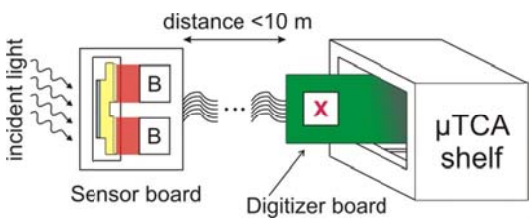

Figure 4: Simplistic view of the detector organization (not in scale).

Figure 4 shows the hardware layout of the detector system. The DAQ board is installed in a µTCA shelf. The sensor board needs to be relatively small in order to make the installation in the FLASH/XFEL diagnostic setups possible. Each Beetle chip has 4 pairs of current mode differential outputs which facilitate using quite long wire connection (up to several meters) between the sensor board and the DAQ board. As a consequence, it is possible to place the digital part of the proposed system in shielded rack. It is worth noticing, that the Beetle chips is designed and fabricated in order to tolerate large radiation dose rates, thus suited for electron beam instrumentation within the accelerator tunnel.

TECHNICAL CHALLENGES

There are several technical challenges involved in the 1 MHz line detector project. The most important is the development and fabrication of the sensor board. The Beetle chip's analogue inputs are organized in four rows. As a consequence, it is necessary to design and fabricate a ceramic epoxy with custom Pitch Adapter using thin-film metallization technique to bond the sensor with the electronics.

SUMMARY

The investigations presented in this paper show that with the described detector architecture, 1 MHz line readout rate with few µs latency is feasible. This goal cannot be accomplished using commercially available products. The actual detector behaviour will be tested with a prototype to prove the concept of the bunch-to-bunch diagnostics based on multichannel sensors.

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