Vector Modulator Card for MTCA-Based LLRF Control System for Linear Accelerators

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***Abstract*—Modern low-level radio frequency (LLRF) control systems of linear accelerators are designed to achieve extremely precise field amplitude and phase regulation inside superconducting cavities. One of the crucial components of the feedback loop is a vector modulator used to drive the high-power RF chain supplying the accelerating cavities. The LLRF control systems for the Free Electron Laser in Hamburg (FLASH) and European X-ray Free Electron Laser (XFEL) are based on the emerging Micro-Telecommunications Computing Architecture (MTCA.4) platform offering numerous advantages for high-performance control systems. This paper describes the concept, design, and performance of the first vector modulator (uVM) module dedicated for RF controls compliant with the MTCA.4 specification developed by PCI Industrial Computer Manufacturers Group (PICMG). The uVM module has been built as a double-width, mid-size rear transition module (RTM) that is accessed by an advanced mezzanine card (AMC). The uVM module incorporates digital, analog, and diagnostic subsystems. The digital part is based on Xilinx Spartan 6 family field-programmable gate array (FPGA), with several fast gigalink connections to a control module. The uVM module is equipped with an intelligent platform management interface (IPMI) circuit required by the MTCA.4 standard. The FPGA controls the analog part, which includes fast, high-precision digital-to-analog converters (DACs), In-phase and quadrature modulator chips, programmable attenuators, power amplifiers, and fast RF gates for an external interlock system. The RF chain can be adopted to different carrier frequencies covering a frequency range from 50 MHz to 6 GHz. The design has been carefully optimized for high linearity and low-output signal phase noise. The diagnostic system of the RF chain allows monitoring of input and output power levels and failure detection in the RF circuits. A low-noise and high-performance clocking system makes the uVM a universal device, extending the scope of applications beyond the LLRF control systems. Extensive tests of the board were performed, and the measurement results are presented and discussed in this paper.**

***Index Terms*—Low-level radio frequency, micro-telecommunications computing architecture, rear transition module, vector modulator, xTCA.**

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I. Introduction

THE MODERN superconducting linear accelerator facilities, such as the European X-ray Free Electron Laser (XFEL), use precisely controlled radio frequency (RF) field for electron beam acceleration [1]. The field parameter control is performed by a low-level radio frequency (LLRF) control system [2]–[5] that should ensure up to 0.01% of amplitude and 0.01° of phase regulation accuracy while parallel processing of about 100 RF signals from cavities. Such requirements make the design of the LLRF system a very challenging task that requires using state-of-the-art technology.

The tight field requirements, space constrains, together with high operational availability force the LLRF system designers to build a compact hardware including both powerful digital processing units with Gb/s data transmission, low-latency links, and high-precision RF and analog circuits. Commonly used hardware standards like VERSAmodule Eurocard (VME) or PCI eXtensions for Instrumentation (PXI) [6] exhibit serious limitations for such systems as the new LLRF (for example, too slow backplane communication, no hot swap, lack of a hardware management). The new telecommunication hardware standard Micro-Telecommunications Computing Architecture (MTCA) offers modularity, scalability, maintainability, and remote diagnostics capabilities [7]—crucial features for large scientific machines. This standard was adopted for physics experiments requirements, named MTCA.4 [8], and selected as a hardware platform for the Free Electron Laser in Hamburg (FLASH) and European XFEL control systems. The vector modulator described in this paper was designed for this MTCA.4-based control system.

The simplified block diagram of the LLRF system architecture and physical realization in MTCA system of XFEL is shown in Fig. 1. The electromagnetic field used for electron beam acceleration is stabilized in superconducting cavities operating at a resonant frequency of 1.3 or 3.9 GHz. High-frequency input and output signals of accelerating cavities are converted down to an intermediate frequency (IF) by multichannel downconverter modules (DWC) designed as rear transition module (RTM) cards. IF signals are analog-to-digital converted by an advanced mezzanine card (AMC) digitizer module.[1] Data from up to eight digitizer modules are collected by the main LLRF controller module (uTC) realized as an AMC card [9] using low-latency links (LLLs) available on the AMC backplane [10]. Complex real-time controller algorithm running on a powerful field-programmable gate array (FPGA) on the uTC computes the desired output signals that are sent

[1]SIS8300 from Struck Innovative Systems GmbH

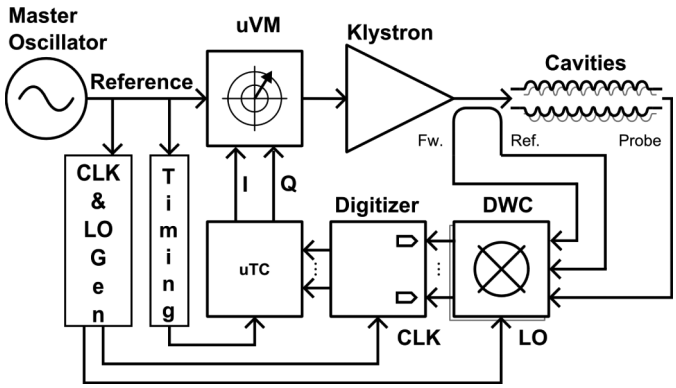

Fig. 1. LLRF system architecture. The vector modulator (uVM) is an actuator, and uTC is a controller in the feedback loop.

to the RTM vector modulator module. At the uVM, the digital data is deserialized and converted by fast digital-to-analog converters (DACs) to drive in-phase and quadrature (IQ) inputs of a modulator chip. The LLRF system feedback loop is closed by driving a high-power klystron supplying up to 32 accelerating cavities. The performance of the vector modulator is one of the factors limiting the performance of the entire LLRF system. Therefore, the uVM design must incorporate low-noise and high-performance analog chain. On-board diagnostics and high-availability technologies are required as uVM's operation reliability is crucial for the overall system availability.

The uTC AMC board interfaces directly with the uVM card by the Zone 3 connectors with a low-latency gigabit link. This is a unique feature of the MTCA.4 standard allowing interfacing physically separated high-performance analog and digital modules in a modular, hot-swappable, and fully managed system.

The uVM module has been designed to fulfill stringent requirements of the FLASH and XFEL control systems and to provide additional diagnostic and interlock functionality in a very compact RTM format [8]. For systems requiring lower computational power and less channels, the uVM can be interfaced with a low-cost AMC card. The uVM module also supports an RF Backplane (uRFB [11]) that can be added to the MTCA.4 crate in order to significantly reduce the RF cable connections and improve the maintainability of the electronic crate system.

II. Requirements for Vector Modulator

A. Functional Requirements

Integration with LLRF system is ensured by the following:

- data links between the controller and the uVM. Minimum 10 bidirectional, differential pairs are required;
- compatibility with uRFB.

The vector modulator module should support a standalone mode of operation and actuator mode. The standalone mode is suitable for debugging, quality control, and measurements of the uVM board. In the closed feedback system, the uTC serializes and sends calculated IQ drive signals to the vector modulator card through the Zone 3 connector using a gigabit link [13]. The link should introduce latency below 200 ns [10]. The uVM card is responsible for performing a single sideband modulation with a deserialized modulating signal in two independent but identical channels. In the LLRF system, the first channel is used for driving the klystron, and the second for system calibration.

The input and output power of the RF signals should be monitored (in digitized format) for failure detection. The output signals can be turned off in emergency situations with a low-latency RF switch called the RF gate. SMA connectors for input and output signals should be mounted on the front panel.

Clocks for the converters and the FPGA can be synthesized on-board using the RF input signal as a reference or provided externally either over the RF backplane or front-panel SMA connector.

B. Electrical Requirements

Each channel should provide signals with at least a power level of $+10$ dBm, and a discrete attenuator from -15 to 0 dB with 5-bit resolution (while maintaining full I and Q resolution) controlled by the software. The desired RF channel crosstalk should be -70 dB, not to exceed nonlinearity errors of the affected channel. The baseband IQ signals should be low-pass filtered with a corner frequency of 50 MHz before entering the modulator chip input. Differential signals are preferred for all types of communication and analog connection because of their better noise immunity and resistance to electromagnetic interference compared to single-ended signal channels.

C. Requirements for European XFEL

The European XFEL requires extremely stable amplitude (0.01%) and phase (0.01°) regulation of accelerating field in order to provide a bunch arrival time jitter of less than 60 fs (all values RMS). Detailed analysis of the phase noise budget for the LLRF system can be found in [14]. Precise regulation performance determined by the strong requirements on beam stability demand a highly accurate up-conversion of processed control signals. Proportional gain factor of a complex multiple-input–multiple-output (MIMO) controller at low frequencies, maximum pulse duration, an iterative learning control algorithm, and trigger signal synchronized to mains reduce repetitive distortions in a frequency range below 1 kHz. Due to the effective closed-loop bandwidth of the LLRF system for superconducting cavities of about 40 kHz within the current setup, contributions from vector modulator noise must be minimized within this frequency range. Filtering within the LLRF control algorithm, preventing excitation of additional resonant modes of the cavity, might lead to a field effect unobservable by the control system, but disturbing the electron bunch. Therefore, no distortions can be added by the uVM in the frequency range up to 4 MHz.

In order to achieve the desired field amplitude and phase stability, the following electrical requirements have been put:

- nonlinearity on IQ plane $\leq 0.1\%$;
- short-term noise ≤ -160 dBc/Hz (above 1 MHz offset); IQ plane nonlinearity is defined as maximum magnitude ratio of error vector to ideal full-scale signal over full phase range [15].

D. Other Requirements

The vector modulator module should fulfil the following requirements concerning the MTCA.4 standard:

- double-width, mid-size AMC form factor RTM [8];
- hot-plug switch and LEDs required by Intelligent Platform Management Interface (IPMI) standard [12] on the front panel;
- management and diagnostics according to IPMI standard

III. Design Description

A. Previous Designs

Single sideband modulation has been traditionally realized by two methods—filtering and phasing [16]. Undesired sideband can be filtered out. Filters with very steep frequency characteristics are required to achieve good sideband and carrier suppression. Design of filters for modulation frequencies of tens of hertz and carrier frequency in the gigahertz range in a compact form factor is not possible since filter order would be very high [17].

In the phasing approach, no filters are needed, as the output signal is a combination of IQ carrier signals modulated (respectively) by the input signal and its Hilbert transform (for sinusoidal modulation, it is equivalent to a phase change of 90°) using balanced mixers [18]. An architecture using two frequency synthesizers generating modulated signals has been proposed in [19], but phase truncation in direct digital synthesis logic circuits can result in spurs in the ouput spectrum. For this system, modulated signals cannot be generated directly by DACs due to their frequency range spanning above the currently available DACs' output bandwidth.

Taking into consideration the desired phase noise level, the linearity and the modulation signal bandwidth IQ modulator has been chosen. Instrumentation Technologies[2] has designed an AMC vector modulator card [20] combining the functionality of the vector modulator and the controller cards, but performance evaluation of the RF modulation chain has not been published.

Realization of a vector modulator board working in an ATCA-based LLRF system has been described in [21]. That device is a full-size AMC module composed of two printed circuit boards (PCBs) connected using a 120-pin high-speed connector. It occupies two parallel slots and has only one RF channel.

No data are available for direct comparison, but taking into account the performance of IQ modulator chips offered by leading semiconductor manufacturers (Hittite, Analog Devices, Texas Instruments), meeting the requirements given in Section II-C presents a significant challenge for the designers, and the module described in this paper reaches the performance limits of current technology.

B. Analog Subsystem

Key components of the analog part of the uVM module have been identified by the requirements described in Section II-A. Based on given functional and electrical requirements, a structure of analog subsystem has been proposed.

[2]http://www.i-tech.si/

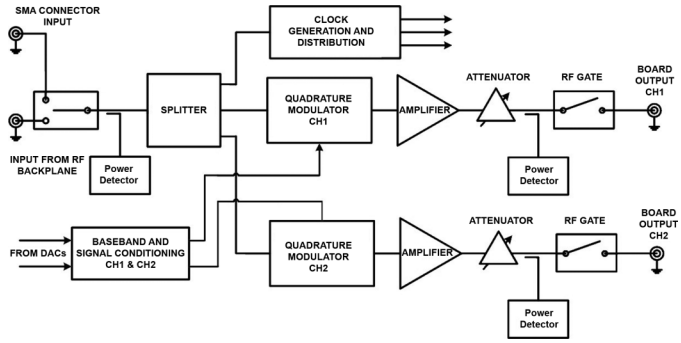

Fig. 2. Block diagram of the analog subsystem of the vector modulator card.

The block diagram of the vector modulator board's analog part is presented in Fig. 2. The RF switch selects the input signal either from the SMA front-plate connector or from the uRFB. The switch is controlled digitally by the FPGA, and therefore the signal source can be selected online by the system control software. The power splitter distributes the RF reference signal to two independent modulator channels as well as to the clock generation and distribution circuit. Each RF chain is composed of an IQ modulator, an amplifier, a programmable attenuator, and an output gate. DACs generate baseband analog signals driving the IQ modulator chips. Three power detectors monitor input and output signal power. Detailed considerations on each block will be provided in the following paragraphs.

1) RF Chain: The principle of the operation of an integrated IQ modulator has been described in [22], including linear and nonlinear errors. It simultaneously controls amplitude and phase of the output RF signal. Such chips are widely used in wireless communication because they can be used to realize any digital modulation scheme.

Signal modulation chains should be optimized for achieving low noise floor, low-linear and nonlinear distortions, as well as coupling of external signals for optimal LLRF system performance.

The most important element of each RF channel is the IQ modulator. The parameters of the modulator have the most significant impact on the chain performance. A low-noise, wideband, high-linearity integrated circuit with matched input and output impedances has been selected.

Output signal's nonlinearity can be considered in the aspect of nonlinear signal driving the modulator and odd orders intermodulation distortions. Linearity of the modulating IQ signal is determined by the performance of the selected DACs and the designed signal conditioning circuit. Intermodulation distortions have been minimized by choosing the optimum operation point of the modulator chip and amplifier. The level of harmonics of the carrier signal at the output and their modulation have been considered unimportant to this project due to narrowband operation of the klystron.

The modulator chip, which is the first element of each RF channel, determines the noise floor achievable for the entire chain. The signal-to-noise ratio is slightly (0.5 dB) deteriorated by following elements of the chain.

To meet the desired power level, a low-noise, linear RF amplifier delivering a power of $+15$ dBm has been used. Such level

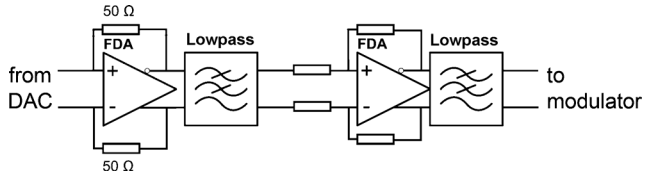

Fig. 3. Block diagram of the baseband signal conditioning chain.

has been selected to ensure maximum power level of +10 dBm at the board output.

The attenuator can provide attenuation in the range of 0–15.75 dB, digitally controlled in 0.25-dB steps.

A logarithmic power detector with a 70-dB dynamic range and high linearity (1 dB error over 60-dB range) converts the input RF signal to a proportional dc voltage. This signal is low-pass filtered (with a corner frequency of 48 Hz) and amplified to match the full scale of an analog-to-digital converter.

Compatibility with the uRFB is provided by two connectors—one multicoaxial (RF reference input) and one multiple differential pairs (analog power supply and clock).

2) Baseband Chain: High-resolution (16-bit), fast (160 MSPS) DACs generate baseband differential analog IQ signals.

Selected DAC chips have two independent, complementary current-source outputs each with full-scale current set by an external resistor and software. Such outputs achieve best linearity when working in constant voltage mode. The compliance range of the DAC and the common mode of the modulator chip do not allow interfacing them directly.

Therefore, a two-stage baseband signal conditioning circuit has been designed (block diagram visible in Fig. 3). The first stage performs complementary current-to-voltage conversion (preserving constant voltage at the DAC output) and low-pass filtering, while the second amplifies the signal, filters it, and changes its common mode (set by another DAC). The imbalance of the whole baseband chain and inputs of the modulator can be calibrated using software capabilities of the main DAC to control the amplitude and offset on each channel.

3) Clocking: Another factor influencing the modulated signal's quality is the spectral purity of the signal clocking DACs. Therefore, high-performance clock generation and distribution components have been used. The clock can be generated by frequency division of the RF reference signal or distributed directly by a specialized 10-output chip (6 LVPECL and 4 LVDS).

4) Power Supply: The digital circuits can be powered directly by single stage dc/dc converters. The analog part requires a two-stage supply with additional low-dropout, low-noise analog regulators and suitable passive filtering. Improved RF quality substrate material has been chosen as a compromise between price and performance.

C. Digital Subsystem

The digital subsystem of the uVM module is composed of the Spartan 6 FPGA device, power supply unit, and IPMI management circuitry required by the MTCA.4 specification. The

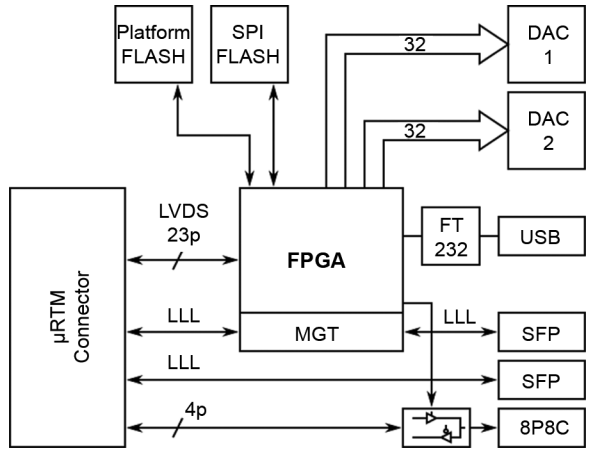

Fig. 4. Block diagram of the digital subsytem of uVM.

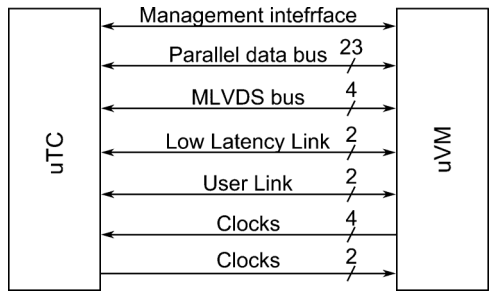

Fig. 5. uVM Zone3 interconnections block diagram.

block diagram of the digital part is presented in Fig. 4. The uVM FPGA controls the main DACs, clock distribution circuit, attenuators, RF power monitoring circuit, monitoring analog-to-digital converters (ADCs), and baseband DACs. The device can be controlled using diagnostic USB interface available on the uVM face-plate when operating in standalone mode.

The uVM module communicates with the uTC board using digital signals only. The Zone 3 connector provides two low-latency serial connections (the LLRF and user interfaces) and parallel, general-purpose low-voltage differential signaling (LVDS) signals; see Fig. 5. The low-latency connections provide data transmission with latency lower than 150 ns with a maximum 3.125-Gb data throughput. One of the low-latency serial connections is used as a main data transmission channel between uVM and uTC. The second high-speed serial link is provided between the uTC FPGA and the small form factor pluggable (SFP) transceiver available on the uVM faceplate. This LLL connection can be used for connecting to other LLRF subsystems using an optical fiber. In addition, four LVDS signals are available on the uVM face-plate via 8P8C modular jack. These signals can be used to connect additional subsystems of the LLRF control system, e.g., Lorentz Force Detuning compensation module. The LVDS signals are used for the FPGA in system programming and FPGA PROM firmware upgrade [23].

1) Module Management: The MTCA.4 standard requires system for RTM management and diagnostics. The subsystem is used for module activation, deactivation during the hot-plug

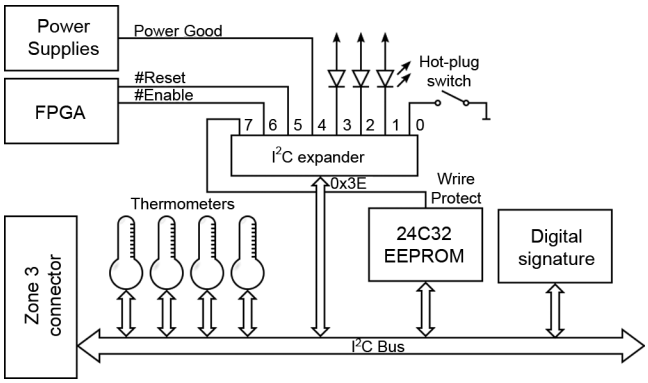

Fig. 6. Block diagram of the module management subsystem.

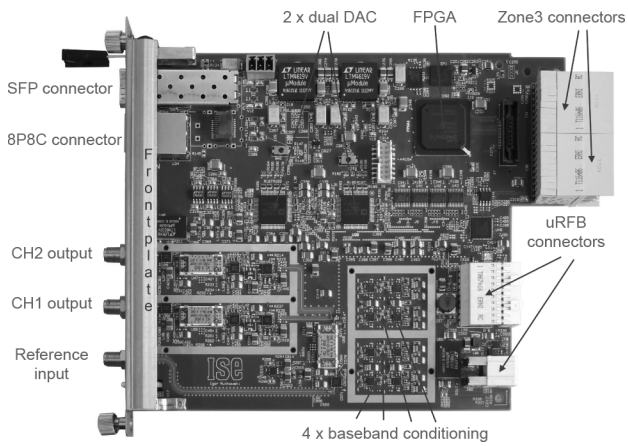

Fig. 7. Assembled uVM card.

procedure, and temperature and voltages monitoring. It provides also field replaceable unit (FRU) hardware description according to the IPMI standard [12].

The uVM board is equipped with basic management and hardware monitoring, as illustrated in Fig. 6.

The subsystem is based on an 8-bit I^2C expander. It is responsible for reading the hot-swap sensor, driving optical indicators required by the IPMI standard, and monitoring power-supply diagnostic signals. It also provides a two-wire interface to the FPGA and controls the "write protect" signal of the on-board serial EEPROM memory. The EEPROM is used to store FRU information describing the RTM module capabilities according to IPMI and AMC standards. The board is equipped with four MAX6626 thermometer chips placed in the most critical parts of the uVM board. In addition, every uVM board has a unique 64-bit digital signature.

D. PCB Design

A 10-layer PCB was designed for the uVM card. Geographical partitioning technique was applied to reduce unwanted spurious polluting the analog part due to common return currents path and excessive voltage drop in ground conductors. The microstrip transmission lines were used, reducing signal power losses.

The photograph of the designed device is shown in Fig. 7. The most important components are marked, including the FPGA, connectors, DACs, and baseband conditioning circuits.

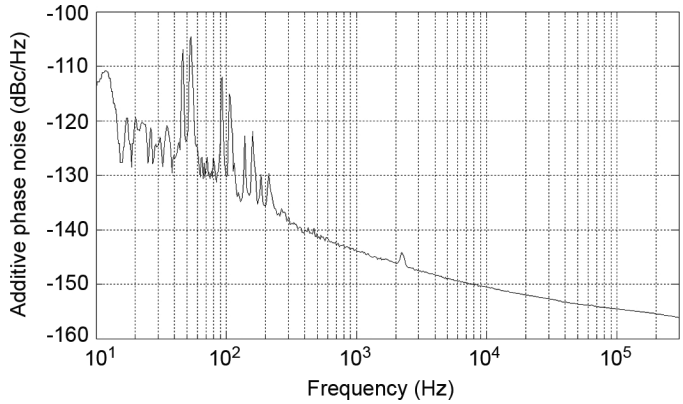

Fig. 8. Additive phase noise spectrum of the vector modulator card.

TABLE I
INTEGRATED PHASE NOISE CONTRIBUTION PER DECADE.

Frequency band (Hz)	Additive jitter (fs RMS)
10 - 100	1.7478
100 - 1k	0.7695
1k - 10k	0.4883
10k - 100k	0.8561
10 - 100k	2.6527

IV. TESTS

Extensive laboratory tests have been performed on the vector modulator module. First, the uVM module has been configured for operation in the standalone mode. An external computer has been used for configuration of components of the uVM module.

A. Analog Subsystem Tests

The additive phase noise of the uVM board has been measured using Blue Phase 1000 [24] from Wenzel Associates with an oscillator generating 1.3-GHz signal with very low noise floor (– 180 dBc/Hz at 20 MHz offset) being the RF reference signal. I and Q signals have been set to constant, maximum values.

Spectrum of output signal has been presented in Fig. 8. Strong peaks around frequency 50 Hz and its harmonics are visible, but the additive phase noise of the device above 250 Hz is very low. Total contribution per decade has been calculated and presented in Table I. Integrated phase jitter in a band 10 Hz–100 kHz (limited by the test system corner frequency) is 1.24 mdeg (2.17E-5 rad). Achieved performance leaves an 18-dB margin from the desired arrival time jitter for the rest of the system components.

For maximum module performance [22], the calibration of the modulator chip channel asymmetry and offsets has been performed by manual tuning of offsets and gains on each baseband I and Q channel while applying a modulation of the input signal with a complex sine wave, following a procedure described in [25]. After the calibration has been performed, power levels of the carrier, sidebands, and their harmonics have been measured, and the results are presented in Table II. Channel 2 linear errors (carrier leakage and unwanted sideband suppression) level meets the requirement presented in Section II-C by a small margin, but fidelity of the signal at channel 1 output is

TABLE II
SPECTRUM OF THE MODULATED SIGNAL

Harmonic	Ch 1 Power [dBm]	Chl 2 Power [dBm]
3	-50.77	-49.75
2	-49.66	-50.82
Wanted sideband	15.26	15.16
Carrier	-46.75	-58.52
Unwanted sideband	-33.48	-45.24
-2	-44.33	-46.87
-3	-16.43	-18.09

not sufficient. Channel 1 unwanted sideband suppression and carrier leakage errors levels are roughly equal to the worst-case performance of the IQ modulator chips guaranteed by the manufacturer.

B. Digital Subsystem Tests

The digital connections have been tested when the module has been installed in a 12-slot Elma chassis [26] equipped with a MicroTCA Carry Hub (MCH) from NAT [27] and an AMC-1000 card from Adlink [28]. The uVM has been connected with the uTC module (revision 1.3) [9]. The main FPGA of the uTC module sends data with a CRC checksum using two LLL and all available LVDS channels. The FPGA available on the uVM module receives data and calculates CRC. When a mismatch in CRC is detected, a suitable error counter for tested link is incremented. The calculated bit error rate (BER) for LLL working with 3.125 Gb/s is below $2 \cdot 10^{-14}$ bits.

V. CONCLUSION

The design of an MTCA.4 compliant vector modulator module is described in this paper. It is realized by a two-channel RTM module designed for RF operation in a broad signal frequency range between 50 MHz and 6 GHz. The uVM module incorporates a Spartan 6 FPGA used for fast communication with AMC modules and for driving 16-bit, 160 MSPS DACs. Auxiliary features have been added, like on-board programmable attenuators, an RF-gate for fast interlock, and monitoring circuits. The board has been physically split to analog and digital parts, and RF design techniques have been applied for the optimization of modulator parameters.

The digital part of the uVM module provides management and diagnostics functionality required by the MTCA.4 standard. The Zone 3 connector allows transmitting data with latency lower than 200 ns that fulfills the LLRF requirements. The FPGA device provides additional processing power for data post-processing and controlling the DAC chains.

Extensive tests described in the paper prove the high performance of the designed board. The piece-to-piece variation of IQ modulator chips' characteristics is an important factor limiting nonlinear performance of the design. The various features added to design of the uVM module make this module a very universal and powerful device suited not only for the LLRF system but also for other RF signal processing applications.

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