Outline

> Review regulation concept within pulsed operation mode

> Identification of control applications to be migrated
  - Hardware modifications
  - Software modifications
  - Issues using VS control

> Changes required in DAQ and control

> Final remarks
General changes to our current approach

> Higher loaded quality factor => lower bandwidth of the system

- $Q_l = 3e7$ corresponds to 43Hz (full bandwidth) @ 1.3GHz
- Changed objectives in the controller design
- Higher susceptible to cavity resonance frequency change

> Ramping the cavity to a steady state operation point

- Possible scanning ranges, frequent operation point changes ?
- Cavity detuning is dominated by stochastic rather then predictive components
- Reactive compensation, some oscillations might be predictable but with possible phase changes

> Learning from previous pulses not possible

- Steady state errors must be compensated from feedback (integral term)
- Controller design goal changes from disturbance rejection more to reference tracking
- Design methods to be essential, filtering more elegant
Control and automation applications migration

> Pulse to pulse adaptations

- Iterative learning control (LFF), other approach using frequent disturbance suppression
- A-priori information distribution (bunch pattern)
- Output vector correction (Drift within the driving chain)
- DAC offset correction (OP depending)
- Lorentz force detuning compensation

> Limiters and calibration

- Signal limiters (no waveforms)
- Quench detection (online FW)
- Vector Sum (individual cavities)
- Beam phase calibration
- Virtual probe calculation

> Statistic and diagnostics

- Simple QI /detuning measurement
- System performance evaluation
MicroTCA.4 LLRF VS control – signal flow
Hardware changes

> Drift compensation module (DCM)

- From pulsed to two tone calibration method (couplers instead of switches)

> MicroTCA.4 cards

- Single cavity / vector sum controller (depending on the control strategy / amplifier)
- CPU?, data reduction, changed DMA request frequency
- Processing power requirements to the FPGA
The resonance peaks bandwidth scale with changing of QI (higher)

- Shifting with microphonics as the acceleration mode

Setup of filters and identification of the mode might get more delicate

- Stability areas and delays have to be qualified
Example: Beam loading compensation

- Requires pre-compensation of the expected beam induced field drop
  - Delay in the transmission and detection (compensating the contribution perfectly requires a-priori knowledge of the beam)
  - True for begin and end => delay shifted compensation
  - Exact beam charge is not known, given beam pattern might very from requested
  - Information can be based on previous bunches (repetitive and slow drifts)
Issues induced by vector sum control in CW

Calibration errors sensitive to microphonics

- Averaging (stochastic), problematic if frequent/beam repetitive errors
- Expected lower accuracy (bunch repetition range is lower - SNR)
- Alternative method of calibration, no fundamental change
Microphonic challenges

- Harmonic and stochastic microphonics
  - Distribution along cavities or modules (phase advance)
  - Mechanical response on the individual cavities
- Single cavity regulation or vector sum control (cavity coupling)
Ponderomotive instabilities (pre-detuning)

- In VS operation could lead to collective excursions
  - How to disentangle cavities?
  - Pre-detuning goal might differ from minimum detuning in steady state

- Requires fast and sophisticated treatment of excursions
  - Fast piezo movement if peak is reached
  - Operation stability margin

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<th>$V_{\text{max}}$ MV m$^{-1}$</th>
<th>$V_{\text{ave}}$ MV m$^{-1}$</th>
<th>$P_{\text{max}}$ kW</th>
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Piezo control essential

- Depending on loaded Q and also on detuning expected
- Distinguish between repetitive, stochastic and static frequency offset contribution

  - Mechanical tuners are too slow, also permanent movement is not wanted
  - If no piezo, the effects induced by the detuning have to be compensated by the controller itself
  - This puts additional effort to the controller (high gain, also high feedback of induced measurement errors, but HF contributions are even better suppressed by lower cavity bandwidth)
From long pulse to CW

> Ramping routine might be an issue

- Self excited loop, generator driven excitation
- Frequency modulation (RF) or maintaining the resonance frequency (PZT)
- Predictable detuning waveform can be applied (mechanical model of the system)

> Switching transition required (ramping to continuous)

- Control objectives might be different for both stages
- System behavior might differ => switching controller vs. performance
Acquiring and processing of data

> So far 1% duty cycle => long time for transmitting and processing
  - Ideally we could have a continuous data stream (contradiction with long pulse mode)
  - Double buffering inside firmware registers
  - DAQ and control tables could be flexible (single floats)

> No dedicated waveforms required for CW operation but
  - Ramping procedure (how to reach steady state conditions)
  - Frequent (cw) beam loading compensation (predictive)
  - Frequent compensation of detuning (ANC)
  - Frequent disturbance rejection (pzt, others?)

> Since more processing is done in FW, less information is to be send to the CPU, data reduction, data exchange frequency to be decided

> Amount of data stored in DAQ (CW not possible to store current amount)
Final remarks

> CW might also mean frequent ramping, stepping for multiple beamlines
  - As it is in long pulse, the pulse (data) length is not defined (must be dynamic 1…x)

> Interfaces to other subsystems
  - Additional interlocks required?

> Review of our internal safety features
  - Limiters, reaction on QI changes, fast detuning detection and reaction

> Loading of control tables and data acquisition
  - Flexible solution with cw, long pulse (variable) leads to more generic solution

> Beam based feedbacks / disturbances
  - Repetitive patterns, a-priori information

> Optimal controller design requires likely more sophisticated controller structures
  - Additional FPGA resources

Thanks for your attention.
LLRF digitalization and data processing

1. RF signals are down converted to an IF of 54 MHz
2. ADC sampling with 81 MHz + adjustable delay in steps of 1/81 MHz
3. IQ detection and averaging over 9 sampling points
4. Further data processing with 9 MHz