Production errors & improvement of our quality standards

Quality Management for XFEL Series Production

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Warsaw, 10.06.2014
> Development focus is on design
> Challenge: Series production
> Observations:
>   - Mistakes are discovered in “Production revision"
>   - Issues forgotten in new revision
>   - Problem with reproducibility and repeatability
>   - Difficult to find data (“final?”)
>   - No History
> Simple mistakes are difficult to handle if we have 50+ Boards and 50,000+ Euro costs
Use SVN for design data storage

Provides backup, sync., traceability, history, freezing

“Living” files (Altium, mechanics, firmware) go to SVN

“Dead” data (e.g. data sheets, measurement data) go to N drive

Do not put trash (e.g. temp) files there to SVN

Commit regularly (e.g. every day), use a verb in commit text

Each Project shall have branches, tags and trunk
  • Trunk is the design in progress
  • Tag: Create it whenever a board arrives (for each physical board we shall have a tag)
  • Branches: Are different versions and modifications (e.g. FRED3M)

https://svnsrv.desy.de/basic/MSK_PROJECTS/
https://svnsrv.desy.de/basic/MSK_HVF-PROJECTS/
Development Framework

> Use Altium Vault as the only library for new (!) designs
  - Clean library can avoid manufacturing issues, reworks and redesigns
  - Provides traceability and history and update of faulty components
  - Provides clean BOM and Assembly plots with no extra effort
  - Managed by Robert (applies common rules)
  - Adoption of shared library is an iterative process.

> Laboratories
  - Order replacement when you use something up!
  - We will install a list of missing things that have to be ordered
  - If you take something away, please leave a note
  - JTAG adapters are now personal – do not steal them
Design

➢ Schematics
  ▪ Please use proper templates and deliver clean schematics.
  ▪ Use comments in schematics. (Avoid red color for comments)
  ▪ Do ERC and review the problems
  ▪ Define all components, at least by „best guess“ – no „undefined“ parts

➢ PCB
  ▪ Boards shall have no DRC mistakes (sometimes very few are acceptable)
  ▪ Prepare fabrication information.

➢ Variants: Keep Number of Variants as low as possible. Document Differences
Production – Many issues because of non-precise data

➢ Please review all the production files.
  ▪ Avoid unnecessary files. All has to be consistent & correct.
  ▪ Include impedance, material, surface information.

➢ Review BOM. Provide exact manufacturer and part number
  ▪ Ordering numbers are optional. If you have them, make sure they are correct.
  ▪ Mark components that can be replaced with generic ones.

➢ Provide assembly drawing as PDF !!!
  ▪ Usually 4 pages (Designators and values top/bottom) - Check Pin 1 Marking!
  ▪ Include Manufacturer instructions. (e.g. hand soldering)

➢ Board shall come from one hand
  ▪ Ask assembly company to order parts and PCB.

➢ TAG received Boards
Assembly drawing

Board Thickness: 1.6mm
Layer Count: 6
Layer Stack-up According to attachment
Board Material: Standard FR4
Smallest Track: 100um
Smallest Hole: 0.2mm
Surfaces NE/Pb
Print Overlay (Silkscreen): no
Board Outlines Milled
Impedance: Only Layer 5, differential 100 Ohm
100R Configuration: Diff. 80Ω 450-100/100-100, see attachment
Impedance Measurement report required: yes

CONFIDENTIAL MATERIAL

DFMC-SFP4
Top Designators

DESY
Hamburg
2015

DESY reserves all rights according to ISO 16016.
Board Testing

> Minimum: Check operation of all ICs (indirect check also ok)
> Report problems in Redmine
> Use stickers for marking boards (green/yellow/red/brown)

### Tracker

<table>
<thead>
<tr>
<th>#</th>
<th>Tracker</th>
<th>Status</th>
<th>Priority</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>1495</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>Isolating Tape needed on green LED unter FP Mechanics</td>
</tr>
<tr>
<td>1494</td>
<td>Improvement</td>
<td>New</td>
<td>Normal</td>
<td>Rotate all Texts on PCB to be readeble when in crate</td>
</tr>
<tr>
<td>1493</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>DCDC Switching Frequency is too low</td>
</tr>
<tr>
<td>1492</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>Modification for IPMI access from CPLD</td>
</tr>
<tr>
<td>1491</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>Ground unused MCU pin for revision detection</td>
</tr>
<tr>
<td>1490</td>
<td>Improvement</td>
<td>New</td>
<td>Normal</td>
<td>DDR2 memory differential clock termination wrong</td>
</tr>
<tr>
<td>1396</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>Front Panel Holes for Light Pipes are too big</td>
</tr>
<tr>
<td>1393</td>
<td>Bug</td>
<td>New</td>
<td>Normal</td>
<td>FMC1 presence pullup is wrong</td>
</tr>
</tbody>
</table>

### FMC25 Test Report

<table>
<thead>
<tr>
<th>Region</th>
<th>Design Test</th>
<th>Value/Result</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>JTAG Accessibility of Virtex-5</td>
<td>works at 12 MHz</td>
<td>verify with JTAG at 12 MHz</td>
</tr>
<tr>
<td>FPGA</td>
<td>PCIe function</td>
<td>PCIe works</td>
<td>verify with application</td>
</tr>
<tr>
<td>FPGA</td>
<td>P2P Links</td>
<td>test all links</td>
<td>put 2 boards in crate, verify with BERT, note BER</td>
</tr>
<tr>
<td>FPGA</td>
<td>MLVDS Links</td>
<td>Toggle Levels</td>
<td>at max rate with FPGA, verify with scope</td>
</tr>
<tr>
<td>U9</td>
<td>Reference Voltage</td>
<td>2.49V</td>
<td>verify with scope, note voltage level</td>
</tr>
<tr>
<td>U19</td>
<td>JTAG Accessibility of Spartan-3</td>
<td>works at 12 MHz</td>
<td>verify with JTAG at 12 MHz</td>
</tr>
<tr>
<td>CPLD</td>
<td>JTAG accessibility</td>
<td>works at 12 MHz</td>
<td>verify with JTAG at 12 MHz</td>
</tr>
<tr>
<td>USB</td>
<td>SPI Flash</td>
<td>works</td>
<td>program FPGA image at max config rate and max bus width</td>
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<td>USB</td>
<td>SPI Flash</td>
<td>works</td>
<td>program FPGA image at max config rate and max bus width</td>
</tr>
<tr>
<td>USB</td>
<td>Communication with MMC, SPI</td>
<td>works at 115200</td>
<td>verify simple Communication with Terminal</td>
</tr>
<tr>
<td>USB</td>
<td>Return for IPMB</td>
<td>works</td>
<td>Generate File and Download our bins to SVN</td>
</tr>
</tbody>
</table>
Mass production is a challenge

We have to improve our procedures and production files to manage this

We need traceability

Use our framework (SVN, Redmine, Vault) - the team will benefits.
Requirements for Technosystem

- Do not produce a board where an assembly drawing is missing
- Do not use silkscreen for component orientation
- Replace only components marked as generic/multicomp
- Request confirmation when changing non-generic parts
- Stop if board delaminates
- Provide an error report for each batch
- Do a simple visual check on all the boards
One Correction

- 200mVpp ripple coming out of each Voltage input on FRED2A, FRED2B.
- Solved in FRED2C, FRED3x.