Current state

- No activity since Samer left

- Schematics reviewed and simplified
  - Lower hierarchy levels → changed digital power distribution
  - CPLD JTAG chain simplified (4 CPLDs)

- PCB under review
  - Many issues left
  - Rule set was not clear; different minimum clearances on different layers
  - Biggest problem: Low number of GND vias
  - Routing of RF traces are sub-optimal
  - Clock distribution in discussion

- Discussion with Manufacturer
  - Ilfa sais they will not manufacture this technology anymore (had problems)
ADC Power Planes

Diagram showing the power plan layout with components like Linear Regulator, Switching Regulator, Intermediate Voltage, 1.9V ADC Main, and various voltage levels like V_{TC}, V_{A}, V_{E}, V_{DR}, and ADC.
RF Signals and Grounding
Place for Heat Sink
Component Collisions
Copper rings of some pads of vias/plated holes too small ~3 mil

Clearance between Zone 3 mechanical key holes and planes too small (~0.2 mm), the pin of the mechanical key must be pressed into the substrate

DDR addresses are on layers SIG6 and SIG7 without any GND - crosstalk, no good reference GND plane

MGT links on Sig9 are too close, impedance problems, cross-talk,

PCle lanes on SIG6 and SIG7 has no reference GND plane on SIG6, if there is plane it is not solid = big problem.

Components are too close to FPGA → Collision, Heat sink?

DDR chips are placed very close, assuming that 3D models Limits us to only one memory manufacturer.

Too small distance between oval hole 12 at left-top corner of PCB. The AMC hot-plug part have sharp edge that will got to PCB substrate and make shortcuts.
Clocking Performance with AD9516

> AD9516 performance not optimal

> The aperture jitter of the ADC is 200fs. = -55 dB = 9 bits

> AD9516 limits to 900 MHz IF input.

> Above this we start losing bits.

> Recommendation is to change to HMC987
Creating space for RF signals