WP02 / WP18 Hardware Overview

Frank Ludwig – DESY
Michael Fenner – DESY
for the LLRF, WP18, HVF Team
Content

- WP02 Hardware Summary
- WP02 Projects (mainly skipped)

- WP18 Hardware Summary I,II,III
- WP18 Projects (mainly skipped)

- Conclusions
## WP02 (current revision, total 33)

**AMC / RTM:**
- DAMC-TCK7 (DM)
- DAMC-DS800 (SH)
- DRTM-KLM1300 (SH)
- DRTM-HOM1300 (SH)
- DRTM-VM2LF (MG)
- DAMC-SIS8300L2 (FL)
- DRTM-DWC10 R11 (DS)
- DAMC-DW8VM1 (MH)
- DRTM-2TCAL (SH)

**AMC / RTM (others):**
- CPU (JB, UM)
- MCH (JB, UM)
- uPWS (JB, UM, FL)
- DAMC-X2Timer (KR, MCS)
- DRTM-X2Timer (KR, MCS)

**Crate / RF-Backplane:**
- eRTM-uLOG1300 (TR, UM)
- MCH-RTM-BM (AR)
- NAT-RTM-PSC (AR)
- RF Backplane (TL, CZ)
- Crate (CZ, UM)

**External 19" Modules:**
- LOGM13 (MZ)
- LOGM39 (MZ)
- DCM13 (JP)
- DCM39 (JP)
- REFM-OPT13 (EJ)
- REFM-OPT39 (EJ)
- REFM-INJ (DS)
- PZ16M (KP, BS)
- PWSM (DK, JB)
- FRED2 (MFE, EJ)
- FRED2 LED Panel (SHA)
- TMCB2 (I-Tech)
- TMCB2 Fixture (DK, ELMA)
- TMCB2 Backplane (STH)

## WP18 (current revision, 17 total)

**AMC / RTM:**
- DAMC-FMC25 (JS)
- DAMC-FMC20 (HTD)
- DRTM-PZT4 (KP)
- DRTM-AD84 (RW)
- DRTM-LASY (EJ)

**FMCs:**
- DFMC-AD16 (RW)
- DFMC-MD22 (RW)
- DFMC-LASIO (MFE)
- DFMC-DSBAM (JS)
- DFMC-SFP4 (MFE)

**Non-standard:**
- Balanced Detector (SY, CS)
- Link Electronic (SY)
- LDD_MEZ (SR)
- LDD_ES (SR)
- LDD_MB2 (SR)
- LDD_MBL (SR)
- LDD-Box (MF, CS)

## RF-Synch, Optics, HVF not included

**Legend:**
- ❌ Not started
- ❌ Specification
- ❌ Re/Design
- ❌ Prototype
- ❌ Debugging needs redesign
- ✔️ Debugging needs no redesign
- ❌ Licensing
- ❌ Pre-production
- ✔️ Documentation
- ✔️ Mass-production
### WP02 Hardware Summary (Status 05/2014)

#### WP02 - Module

<table>
<thead>
<tr>
<th>Responsible Person</th>
<th>Revision</th>
<th>Main reason for delay</th>
<th>Module Usage XFEL</th>
<th>Project Status</th>
<th>Final Revision</th>
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<tr>
<td>DMA-CTC7</td>
<td>2.1a</td>
<td>MMC V1.0 Integration too late</td>
<td>XTIN L1 L2 L3</td>
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<tr>
<td>DMA-DS800</td>
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<td>Mechanical + EMI issues</td>
<td>XTIN L1 L2 L3</td>
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<td>DRMT-CLM1300</td>
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<td>DRMT-HOME800</td>
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<td>DRMT-VMO30L</td>
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<td>DRMT-SIS800L2</td>
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<td>MPC U/G Integration too late</td>
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<td>DRMT-DHC800R1</td>
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<td>Man-power problems</td>
<td>XTIN L1 L2 L3</td>
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<td>DRMT-MBC800M1</td>
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<td>DRMT-ZFCAL</td>
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#### MTCA.4

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<td>Inefficient communication</td>
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<td>MCH</td>
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<td>XTIN L1 L2 L3</td>
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<td>CRMT-MXTimer</td>
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<td>Underestimation of complexity</td>
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<td>CRMT-UXTimer</td>
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<td>Underestimation of complexity</td>
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#### MTCA.4 (other)

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<th>Responsible Person</th>
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<td>RF Backplane</td>
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<td>Mechanical + Discharge</td>
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<td>CRMT</td>
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<td>Mechanical + Discharge</td>
<td>XTIN L1 L2 L3</td>
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#### 19" Modules

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<th>Responsible Person</th>
<th>Revision</th>
<th>Main reason for delay</th>
<th>Module Usage XFEL</th>
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#### 19" Modules (other)

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<th>Responsible Person</th>
<th>Revision</th>
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<th>Module Usage XFEL</th>
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<td>REFQ-15</td>
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#### 19" Modules (other)

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<th>Responsible Person</th>
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<td>REFQ-13</td>
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<td>Man-power problems</td>
<td>XTIN L1 L2 L3</td>
<td>Debugging</td>
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</table>
WP02 – Projects
WP02 AMC/RTM Board Details (Status 05/2014)

Board name / revision: DAMC-TCK7 / 2.0

Boards used in WP/#r: X WP02, □ WP18, total approx. x pieces
Project scheduled: 03/2012 - 06/2014
Responsible Designer: Dariusz Makowski

Board status:
- □ Specification, □ Design, □ Prototype, □ Debugging,
- □ Licensing, □ Pre-production, □ Documentation, □ Mass-production

Board tests status:
- X Laboratory, □ Test-stand, □ FLASH, CMTB, □ by manufacturer
- □ Board support package exists, □ Application firmware exists

Documentation status:
- X Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- □ File structure is adapted from SVN to N group drive
- □ All bugs are reported in Redmine or FailureReports.docx
- □ Test procedures for production defined
- □ Internal manual exists

Working style:
- Board was work-out in a well-defined sequence according to the
- □ Group board design working-plan was used, if not why?
- □ Guideline Design Rules were used, if not why?
- □ A project time schedule plan exists

Current problems:
- □ Unclear requirements, □ Unclear interfaces
- □ Mechanical issues, □ PCB is not fully assembled
- □ PCB rule violations, □ PCB manufacturer problems, □ PCB debugging
- □ EMI PCB problems, □ EMI crate problems
- □ other technical problems:

New revision of board:
- □ Yes, because of

Delay caused by:
- □ Changing requirements during design workflow
- □ Purchase or delivery problems, □ DESY administrative delays, □ Industrial delays
- □ Man-power problems
- □ other reasons:
### WP02 AMC/RTM Board Details (Status 05/2014)

**Board name / revision:** DAMC-DS800 / 1.0

**Boards used in:** WP02: XFEL Lifetime management, XFEL High order Mode detection, CW-Synchronization - 100 PCS

**Project scheduled:** Q2 2014

**Responsible Designer:** Samer Bou Habib

**Board status:**
- [x] Specification
- [ ] Design
- [ ] Prototype
- [ ] Debugging
- [ ] Licensing
- [ ] Pre-production
- [x] Documentation
- [ ] Mass-production

**Board tests status:**
- [x] Laboratory
- [ ] Test-stand
- [ ] FLASH, CMTB
- [ ] By manufacturer
- [ ] Board support package exists
- [ ] Application firmware exists

**Documentation status:**
- [x] Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- [x] Files stored in SVN
- [x] All bugs are reported in Redmine or FailuresReports.docx
- [ ] Test procedures for production defined
- [ ] Internal manual exists

**Working style:** Board was worked-out in a well-defined sequence according to the
- [ ] Group board design working-plan was used,
- [ ] Guideline Design Rules were used,
- [ ] A project time schedule plan exists

**Current problems:**
- [x] Unclear requirements
- [ ] Unclear interfaces
- [ ] Mechanical issues
- [x] PCB is not fully assembled
- [x] PCB rule violations
- [ ] PCB manufacturer problems
- [ ] PCB debugging
- [ ] EMI PCB problems
- [ ] EMI crate problems
- [ ] other technical problems:

**New revision of board:** Yes, because of

**Delay caused by:**
- [ ] Changing requirements during design workflow
- [ ] Purchase or delivery problems
- [ ] DESY administrative delays
- [ ] Industrial delays
- [ ] Man-power problems
- [ ] other reasons:

---

**Actions needed to finish project:**

1. Test and Characterize Rev. 1
2. Migrate to DESY Library
3. Correct Design Rule Violations
4. Make FP, Docs, etc.

**Tests pending:**
- Design Rule Violations
- Mixed Libraries
- Short Circuits

**No Design Review**
WP02 AMC/RTM Board Details (Status 05/2014)

### Board name / revision:
DRTM-VM2LF / 2.2

### Boards used in WP/#:
- [ ] WP02
- [ ] WP18, total approx. x peaces

### Project scheduled:
- 03/2012 - 06/2014/?

### Responsible Designer:
- Igor Runkowski
- Maciej Grzegzółka
- Dariusz Makowski
- Aleksander Mielczarek

### Board status:
- [ ] Specification
- [ ] Design
- [ ] Prototype
- [ ] Debugging
- [ ] Licensing
- [ ] Pre-production
- [ ] Documentation
- [ ] Mass-production

### Board tests status:
- [X] Laboratory
- [X] Test-stand
- [ ] FLASH, CMTB
- [ ] By manufacturer
- [ ] Board support package exists
- [ ] Application firmware exists

### Documentation status:
- [X] Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- [ ] File structure is adapted from SVN to N group drive
- [ ] All bugs are reported in Redmine or FailureReports.docx
- [ ] Test procedures for production defined
- [ ] Internal manual exists

### Working style:
Board was work-out in a well-defined sequence according to the
[Group board design working-plan was used, if not why?]
- [X] Guideline Design Rules were used, if not why?
- [ ] A project time schedule plan exists

### Current problems:
- [ ] Unclear requirements
- [ ] Unclear interfaces
- [ ] Mechanical issues
- [ ] PCB is not fully assembled
- [ ] PCB rule violations
- [ ] PCB manufacturer problems
- [ ] PCB debugging
- [ ] EMI PCB problems
- [ ] EMI crate problems
- [X] other technical problems: Bad assembly (will be corrected soon)

### Actions needed to finish project:
1. New revision need to be tested
2. 
3. 
4. 

### New revision of board:
- [ ] Yes, because of

### Delay caused by:
- [X] Changing requirements during design workflow
- [ ] Purchase or delivery problems
- [ ] DESY administrational delays
- [ ] Industrial delays
- [ ] Man-power problems
- [ ] other reasons:
**Board name / revision:** SIS8300L2

<table>
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<th>Boards used in WP/#:</th>
<th>WP02, WP18, total approx. 300 pieces</th>
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<td>Project scheduled</td>
<td>05/2014 - 08/2014</td>
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<tr>
<td>Responsible Designer</td>
<td>Struck Innovative Systems</td>
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**Board status:**
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

**Board tests status:**
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

**Documentation status:**
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

**Working style:** Board was work-out in a well-defined sequence according to the
- Group board design working-plan was used, if not why?
- Guideline Design Rules were used, if not why?
- A project time schedule plan exists

**Current problems:**
- Unclear requirements
- Unclear interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- Other technical problems:

**Actions needed to finish project:**
1. Prototype
2. Performance verification tests
3. CFT
4. 

**New revision of board:** Yes, because of

**Delay caused by:**
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Power problems
- Other reasons:
  - MMC V1.0 Integration
WP02 AMC/RTM Board Details (Status 05/2014)

Board name / revision: DRTM-DWC10 / 1.1

Boards used in WP/#r: WP02, WP18, total approx. x pieces
Project scheduled: 04/2014 - 06/2014
Responsible Designer: Dominik Sikora

Board status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

Board tests status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style:
- Board was work-out in a well-defined sequence according to the
  - Group board design working plan was used, if not why?
  - Guideline Design Rules were used, if not why?
  - A project time schedule plan exists

Current problems:
- Unclear requirements
- Unclear interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- other technical problems: After validation project is finished

New revision of board:
- Yes, because of

Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrational delays
- Industrial delays
- Man-power problems
- other reasons:

Actions needed to finish project:
1. IQ performance validation
2. S11 improvement validation
3. 700 MHz Operation validation
4.
WP02 AMC/RTM Board Details (Status 05/2014)

Board name / revision: DRTM-DWC8VM1 / 1.1

Boards used in WP/#r:  W02, W18, total approx. 10 pieces
Project scheduled: 06/2013 - 06/2014
Responsible Designer: Matthias Hoffmann

Board status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

Board tests status:
- Laboratory
- Test-stand
- FLASH, REGAE, PIZ
- By manufacturer
- Board support package exists
- Application firmware exists

Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style:
Board was work-out in a well-defined sequence according to the
- Group board design working-plan was used, if not why?
- Guideline Design Rules were used, if not why?
- A project time schedule plan exists

Current problems:
- Unclear requirements
- Unclear Interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- Other technical problems:

New revision of board:
Yes, because of
Several minor bugs/improvements

Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Man-power problems
- Other reasons:

Actions needed to finish project:
1. Correct minor bugs
2. Add recommended improvements (like for DWC10)
3. 
4. 
Board name / revision: DRTM-LOG1300 / 2.0

Boards used in WP/#r: WP02, WP18, total approx. 60 pieces
Project scheduled: 11/2014 - 12/2014
Responsible Designer: U. Mavric / T. Rohley (Sandona Ltd.)

Board status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

Board tests status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style: Board was worked-out in a well-defined sequence according to the
- Group board design working-plan was used, if not why?
- Guideline Design Rules were used, if not why?
- A project time schedule plan exists

Current problems:
- Unclear requirements
- Unclear interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- other technical problems:

Actions needed to finish project:
1. Finalize testing of rev2
2. Pre-production
3. Documentation
4. Mass-production

New revision of board: Yes, because of

Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Man-power problems
- other reasons:

Matching of specific RF sections.
Underestimated complexity of specific sections.
WP02 RF-Backplane Details (Status 05/2014)

Board name / revision: MCH-RTM-BM

Boards used in: WP02 + WP18 RF Backplane Management - 100 PCS

Project scheduled: June 2014

Responsible Designer: Annika Rosner, Michael Fenner, Tomasz Jezierski

Board status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass production

Board tests status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- Files stored in SVN
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style:
- Board was worked-out in a well-defined sequence according to the
- Group board design working-plan was used,
- Guideline Design Rules were used,
- A project time schedule plan exists

Current problems:
- Unclear requirements
- Unclear interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- other technical problems:

New revision of board: □ Yes, because of

Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Man-power problems
- other reasons:

Clear Requirements too late, former Workflow wit N.A.T.
## WP02 RF-Backplane Details (Status 05/2014)

<table>
<thead>
<tr>
<th>Board name / revision</th>
<th>NAT-RPM-PSC</th>
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<tr>
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<td>WP02+WP18: uLOG Power Supply, Piezo Power Supply - 100 PCS</td>
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<td>Project scheduled</td>
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<td>Annika Rosner, Michael Fenner, Tomasz Jezynski</td>
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<tr>
<td>Board status</td>
<td>✓ Specification, ✓ Design, ✓ Prototype, □ Debugging, □ Licensing, □ Pre-production, □ Documentation, □ Mass-production</td>
</tr>
<tr>
<td>Board tests status</td>
<td>□ Laboratory, □ Test-stand, □ FLASH, CMTB, □ By manufacturer, □ Board support package exits, □ Application firmware exists</td>
</tr>
<tr>
<td>Documentation status</td>
<td>□ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual), □ Files stored in SVN, □ All bugs are reported in Redmine or FailureReports.docx, □ Test procedures for production defined, □ Internal manual exists</td>
</tr>
<tr>
<td>Working style</td>
<td>Board was worked-out in a well-defined sequence according to the Group board design working-plan was used, Guideline Design Rules were used, A project time schedule plan exists</td>
</tr>
<tr>
<td>Current problems</td>
<td>□ Unclear requirements, □ Unclear interfaces, □ Mechanical issues, □ PCB is not fully assembled, □ PCB rule violations, □ PCB manufacturer problems, □ PCB debugging, □ EMI PCB problems, □ EMI crate problems, □ other technical problems:</td>
</tr>
<tr>
<td>New revision of board</td>
<td>□ Yes, because of</td>
</tr>
<tr>
<td>Delay caused by</td>
<td>□ Yes, because of Changing requirements during design workflow, □ Purchase or delivery problems, □ DESY administrational delays, □ Industrial delays, □ Man-power problems, □ other reasons: Clear Requirements too late, former Workflow wit N.A.T.</td>
</tr>
</tbody>
</table>

**Actions needed to finish project:**
1. Finalize Requirements Docs
2. Test N.A.T. Hardware
3. Design 100V PM
4. 

---

Collaboration Workshop 2014
Frank Ludwig (DESY) Michael Fenner (DESY)
**WP02 RF-Backplane Details (Status 05/2014)**

**Board name / revision:** RF-Backplane / 3.2

**Boards used in WP/#:** X WP02, X WP18, total approx. 50 pieces

**Project scheduled:** 04/2014 - 06/2014

**Responsible Designer:** T. Lesniak

**Board status:**
- X Specification
- X Design
- □ Prototype
- □ Debugging
- □ Licensing
- □ Pre-production
- □ Documentation
- □ Mass-production

**Board tests status:**
- □ Laboratory
- □ Test-stand
- □ FLASH, CMTB
- □ By manufacturer
- □ Board support package exits
- □ Application firmware exists

**Documentation status:**
- X Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

**Working style:** Board was work-out in a well-defined sequence according to the:
- Group board design working-plan was used, if not why?
- Guideline Design Rules were used, if not why?
- A project time schedule plan exists

**Actions needed to finish project:**
- 1. High-frequency VNA and TDR characterization in DC-6 GHz band
- 2. Recover operation of uRFB automated test stand and its finalization
- 3. Interoperability tests with fully equipped crate (depends on availability of MCH-RTM-BM, RTM-PMs and other modules)
- 4. [They were not available when board was designed]

**Current problems:**
- □ Unclear requirements
- □ Unclear interfaces
- □ Mechanical issues
- □ PCB is not fully assembled
- □ PCB rule violations
- □ PCB manufacturer problems
- □ PCB debugging
- □ EMI PCB problems
- □ EMI crate problems
- □ Other technical problems:

**New revision of board:** □ Yes, because of

**Delay caused by:**
- □ Changing requirements during design workflow
- □ Purchase or delivery problems
- □ DESY administrative delays
- □ Industrial delays
- □ Man-power problems
- □ Other reasons:

Long time for working out MCH-RTM-BM concept (1.5 years!). TL was occupied by other tasks
### WP02 19" Modules Details (Status 05/2014)

#### Module name / revision:
**LOGM-13 / 2.0**

#### Modules used in WP/#:
- WP02, WP18, total approx. 3 pieces

#### Project scheduled:
01/2014 - 06/2014

#### Responsible Designer:
Mateusz Zukocinski

#### Module status:
- Specification
- Design
- Prototype
- Debugging
- Pre-production
- Documentation
- Mass production

#### Module test status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- High Level Software exists
- Application firmware exists

#### Documentation status:
- Production files generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or Failure Reports.docx
- Test procedures for production defined
- Internal manual exists

#### Working style:
- Module was work-out in a well-defined sequence, if not why?
- A project time schedule plan exists

#### Current problems:
- Unclear requirements
- Unclear interfaces
- Unclear rf-power levels
- Mechanical issues
- Problems with optical sections
- Cabling or connector issues
- Internal components are not ready, which one:
  - TMCB2, TMCB2 Fixture, FRED2

#### New revision of module:
- Yes, because of

#### Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Man-power problems
- Other problems:

---

**Actions needed to finish project:**

1. Export of production data
2. TMCB2 fixture STEP models
3. STEP Integration
4. Packaging and Production in Industry
# WP02 19" Module Details (Status 05/2014)

<table>
<thead>
<tr>
<th>Action needed to finish project:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1.</strong> Finishing revision 2.0</td>
</tr>
<tr>
<td>• Designing panels for TMCBv2 and new REDF</td>
</tr>
<tr>
<td>• Designing of the Temperature Controller board</td>
</tr>
<tr>
<td>• Drift calibration accuracy to be checked (firmware)</td>
</tr>
<tr>
<td><strong>2.</strong> Review of rev. 2.0</td>
</tr>
<tr>
<td><strong>3.</strong> Applying changes to rev. 2.1</td>
</tr>
<tr>
<td><strong>4.</strong> Preparing for mass production</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module name / revision:</th>
<th><strong>DCM / 2.0</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Modules used in WP/ftr:</td>
<td>- WP02, - WP18, total approx. 50 pieces</td>
</tr>
<tr>
<td>Project scheduled:</td>
<td>01/2011 - 07/2014</td>
</tr>
<tr>
<td>Responsible Designer:</td>
<td>Jan Plekarski</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module status:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Specification, - Design, - Prototype, - Debugging</td>
</tr>
<tr>
<td>- Licensing, - Pre-production, - Documentation, - Mass-production</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module test status:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Laboratory, - Test-stand, - FLASH, CMTB, - By manufacturer</td>
</tr>
<tr>
<td>- High Level Software exists, - Application firmware exists</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Documentation status:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)</td>
</tr>
<tr>
<td>- File structure is adapted from SVN to N group drive (in progress)</td>
</tr>
<tr>
<td>- All bugs are reported in Redmine or FailureReports.docx</td>
</tr>
<tr>
<td>- Test procedures for production defined</td>
</tr>
<tr>
<td>- Internal manual exists</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Working style:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Module was work-out in a well-defined sequence, if not why?</td>
</tr>
<tr>
<td>- A project time schedule plan exists</td>
</tr>
<tr>
<td><strong>Current problems</strong>:</td>
</tr>
<tr>
<td>- Unclear requirements, - Unclear interfaces, - Unclear rf power levels</td>
</tr>
<tr>
<td>- Mechanical issues, - Problems with optical sections, - Cabling or connector issues</td>
</tr>
<tr>
<td>- Internal components are not ready, which one:</td>
</tr>
</tbody>
</table>

| TMCBv2, FREDv2, Temperature Controller not available yet |
| **Other problems**: |
| - EMI PCB problems, - EMI crate problems |
| - Other problems: |

<table>
<thead>
<tr>
<th>New revision of module:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Yes, because of</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Delay caused by:</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Changing requirements during design workflow</td>
</tr>
<tr>
<td>- Purchase or delivery problems, - DESY administrational delays, - Industrial delays</td>
</tr>
<tr>
<td>- Man-power problems</td>
</tr>
<tr>
<td>- Other reasons:</td>
</tr>
</tbody>
</table>

| DCM v1 fall, TMCBv2 delayed |
### Module name / revision:

**REFM-OPT / 1.0**

### Modules used in WP/#:
- WP02
- WP18, total approx. 12 pieces

### Project scheduled:
01/2014 – 06/??/2014

### Responsible Designer:
Thorsten Lamb, Ewa Janas

### Module status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

### Module test status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- High Level Software exists
- Application firmware exists

### Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

### Working style:
- Module was work-out in a well-defined sequence, if not why?
- A project time schedule plan exists

### Current problems:
- Unclear requirements
- Unclear interfaces
- Unclear rf-power levels
- Mechanical issues
- Problems with optical sections
- Cabling or connector issues
- Internal components are not ready, which one:
  - REFM-OPT PCB, FRED2 – in production
  - TMCB2 – in production??

### Actions needed to finish project:
1. Test of pre-prepared software.
2. Finalize REFM-OPT PCB
   - Version from before introducing changes exists and have been tested – works fine, could be used!
3. ...

### New revision of module:
- Yes, because of

### Delay caused by:
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrational delays
- Industrial delays
- Man-power problems
- Other reasons:
<table>
<thead>
<tr>
<th><strong>Board name / revision:</strong></th>
<th><strong>FRED / 2.0</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>3Boards used in WP/#:</td>
<td>02, WP18, total approx. 100 pieces</td>
</tr>
<tr>
<td>Project scheduled:</td>
<td>design + manufacturing 04/2014 - 05/2014</td>
</tr>
<tr>
<td>Responsible Designer:</td>
<td>Michael Fenner</td>
</tr>
<tr>
<td>Board status:</td>
<td>☐ Specification, ☐ Design, ☐ Prototype, ☐ Debugging, ☐ Licensing, ☐ Pre-production, ☐ Documentation, ☐ Mass-production</td>
</tr>
<tr>
<td>Board tests status:</td>
<td>☐ Laboratory, ☐ Test-stand, ☐ FLASH, CMTR, ☐ By manufacturer</td>
</tr>
<tr>
<td>Board support package exits, Application firmware exists,</td>
<td></td>
</tr>
<tr>
<td>Documentation status:</td>
<td>☐ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual), ☐ File structure is adapted from SVN to N group drive, ☐ All bugs are reported in Redmine or FailureReports.docx, ☐ Test procedures for production defined, ☐ Internal manual exists</td>
</tr>
<tr>
<td>Working style:</td>
<td>Board was work-out in a well-defined sequence according to the Group board design working-plan was used, if not why? ☐ Guideline Design Rules were used, if not why? ☐ A project time schedule plan exists</td>
</tr>
<tr>
<td>Current problems:</td>
<td>☐ Unclear requirements, ☐ Unclear Interfaces, ☐ Mechanical issues, ☐ PCB is not fully assembled, ☐ PCB rule violations, ☐ PCB manufacturer problems, ☐ PCB debugging, ☐ EMI PCB problems, ☐ EMI crate problems, ☑ Other technical problems:</td>
</tr>
<tr>
<td>New revision of board:</td>
<td>☐ Yes, because of NO PROBLEMS 😊</td>
</tr>
<tr>
<td>Delay caused by:</td>
<td>☐ Changing requirements during design workflow, ☐ Purchase or delivery problems, ☐ DESY administrative delays, ☐ Industrial delays, ☐ Man-power problems, ☐ Other reasons:</td>
</tr>
</tbody>
</table>
WP02 19" Sub-Component (Status 05/2014)

**Board name / revision:** TMCB / 2.0

**Boards used in WP/#:** WP02, WP18, total approx. 100 pieces

**Project scheduled:** 06/2013 - 06/2014

**Responsible Designer:** Zarko Lestan (Instrumentation Technologies)

**Board status:**
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

**Board tests status:**
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

**Documentation status:**
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

**Working style:**
- Board was work-out in a well-defined sequence according to the
  - Group board design working-plan was used, if not why?
  - Guideline Design Rules were used, if not why?
  - A project time schedule plan exists

**Current problems:**
- Unclear requirements
- Unclear interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- Other technical problems:

**Actions needed to finish project:**
1. Prototype production
2. FW development/debugging
3. Testing of the boards
4.

**New revision of board:**
- Yes, because of

**Delay caused by:**
- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrative delays
- Industrial delays
- Man-power problems
- Other reasons:
## WP02 19" Sub-Component (Status 05/2014)

### Board name / revision:
**TMCB Backplane / 1.0**

### Boards in WP/#:
- WP02
- WP18, total approx. 100 pieces

### Project scheduled:
11/2013 - 04/2014

### Responsible Designer:
Stanislaw Hanasz

### Board status:
- [ ] Specification
- [ ] Design
- [ ] Prototype
- [ ] Debugging
- [ ] Licensing
- [ ] Pre-production
- [ ] Documentation
- [ ] Mass-production

### Board tests status:
- [ ] Laboratory
- [ ] Test-stand
- [ ] FLASH, CMTB
- [ ] By manufacturer
- [ ] Board support package exits
- [ ] Application firmware exists

### Documentation status:
- [ ] Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- [ ] File structure is adapted from SVN to N group drive
- [ ] All bugs are reported in Redmine or FailureReports.docx
- [ ] Test procedures for production defined
- [ ] Internal manual exists

### Working style:
Board was work-out in a well-defined sequence according to the
- [ ] Group board design working-plan was used, if not why?
- [ ] Guideline Design Rules were used, if not why?
- [ ] A project time schedule plan exists

### Current problems:
- [ ] Unclear requirements
- [ ] Unclear interfaces
- [ ] Mechanical issues
- [ ] PCB is not fully assembled
- [ ] PCB rule violations
- [ ] PCB manufacturer problems
- [ ] PCB debugging
- [ ] EMI PCB problems
- [ ] EMI crate problems
- [ ] Other technical problems:

### New revision of board:
- [ ] Yes, because of

### Delay caused by:
- [ ] Changing requirements during design workflow
- [ ] Purchase or delivery problems
- [ ] DESY administrational delays
- [ ] Industrial delays
- [ ] Man-power problems
- [ ] Other reasons:

### Actions needed to finish project:
1. Final corrections in Altium
2. Production of prototypes
3. Testing of the backplane + board
4. Design & production of mechanical mounting frame (ELMA)

### Ineffective communication
<table>
<thead>
<tr>
<th>Component</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD84 3.0</td>
<td>6x produced and assembled. Ready to use.</td>
</tr>
<tr>
<td>FMC25 3.0</td>
<td>6x produced and assembled. No serious mistakes found. This week assembly of few missing components</td>
</tr>
<tr>
<td>FMC20 2.0</td>
<td>10x produced, 5x assembled. Small mechanical issue, tests on-going</td>
</tr>
<tr>
<td>PZT4 2.0</td>
<td>5x produced, 3x assembled. No major mistakes found, tests on-going</td>
</tr>
<tr>
<td></td>
<td>RTM housing is missing</td>
</tr>
<tr>
<td>AD16 1.0</td>
<td>5x produced and assembled. Functioning, performance test needed.</td>
</tr>
<tr>
<td></td>
<td>Redesign after performance test for 2.5 V version.</td>
</tr>
</tbody>
</table>
- **MD22 2.0**: 5x produced and assembled. Ready to use on FMC20. Redesign for 2.5 V version ready, but not produced.

- **DFMC-SFP4**: Design started, Commercial 900,-€

- **DFMC-LASIO**: Design just started

- **DRTM-LASY**: Design just started

- **DFMC-DSBAM**: 8x produced, one broken, Tests started just before WS?
WP18 Hardware Summary III (Status 05/2014)

- **Balanced Detector:** ?x produced. Ready to use
- **Link Electronic:** ?x produced. Ready to use
- **LDD_MEZ:** 4x V0.0 produced, 1 tested successfully in 26a . Ready to use. Components for 50 pieces existing.
- **LDD_ES:** 36x V1.0 produced and tested. Ready to use.
- **LDD_MB2:** 8x V1.0 produced and tested. Ready to use.
- **LDD_MBL:** not yet designed, discussion/meeting for specs done. Concept clarified and open questions identified. Board will be designed by Sergej.
- **LDD-Box:** not yet designed, discussion/meeting for specs done. Concept clarified and open questions identified. Box designer unclear – Matthias, Cezary
WP18 – Projects
Board name / revision: DAMC-FMC20 / Rev. B

Boards used in: WP18: Optical Synchronisation incl. Motor and Piezo control + communication -- 30 PCS

Project scheduled: Q2 2014

Responsible Designer: Jaroslaw Szewinski, Stefan Korolczuk, Grzegorz Boltruczyk

Board status:
☐ Specification, ☐ Design, ☐ Prototype, ☐ Debugging, ☑ Licensing, ☑ Pre-production, ☐ Documentation, ☐ Mass-production

Board tests status:
☑ Laboratory, ☑ Test-stand, ☐ FLASH, CMTB, ☐ By manufacturer

Board support package exits, ☑ Application firmware exists

Documentation status:
☑ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
☑ Files stored in SVN
☐ All bugs are reported in Redmine or FailureReports.docx
☐ Test procedures for production defined
☐ Internal manual exists

Working style:
Board was worked-out in a well-defined sequence according to the
☐ Group board design working-plan was used,
☐ Guideline Design Rules were used,
☐ A project time schedule plan exists

Current problems:
☐ Unclear requirements, ☐ Unclear interfaces
☒ Mechanical issues, ☒ PCB is not fully assembled
☐ PCB rule violations, ☒ PCB manufacturer problems, ☐ PCB debugging
☒ EMI PCB problems, ☒ EMI crate problems
☐ other technical problems:
Si5338A-A-GMR is EOL

Actions needed to finish project:
1. Fully Assembly + Full Test
2. Teststand
3. Licensing BSP + Demo
4. Documentation

New revision of board: ☑ Yes, because of
☐ Changing requirements during design workflow
☐ Purchase or delivery problems, ☐ DESY administrative delays, ☐ Industrial delays
☐ Man-power problems
☐ Other reasons:

Delay caused by:
☐ other reasons: Mechanical Issue with FMC Modules sticking out by 1 mm
WP018 AMC/RTM (Status 05/2014)

Board name / revision: DAMC-FMC20 / Rev. B
Boards used in: WP18: Optical Synchronisation – 20 PCS
Project scheduled: Q2 2014
Responsible Designer: Hans-Thomas Duhme, Michael Fenner

Board status:
- □ Specification
- □ Design
- □ Prototype
- □ Debugging
- □ Licensing
- □ Pre-production
- □ Documentation
- □ Mass-production
- ✔ Board support package exists
- □ Application firmware exists

Board tests status:
- ✔ Laboratory
- □ Test-stand
- ✔ FLASH, CMTB
- □ By manufacturer
- ✔ Board support package exists
- □ Application firmware exists

Documentation status:
- ✔ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- ✔ Files stored in SVN
- ✔ All bugs are reported in Redmine or FailureReports.docx
- ✔ Test procedures for production defined
- ✔ Internal manual exists

Working style:
Board was worked-out in a well-defined sequence according to the
- Group board design working-plan was used,
- Guideline Design Rules were used,
- A project time schedule plan exists

Current problems:
- □ Unclear requirements
- □ Unclear interfaces
- ✔ Mechanical issues
- □ PCB is not fully assembled
- □ PCB rule violations
- □ PCB manufacturer problems
- □ PCB debugging
- □ EMI PCB problems
- □ EMI crate problems
- □ Other technical problems:

Actions needed to finish project:
1. Full Rev. B Test
2. Teststand
3. Licensing BSP + Demo
4. 

New revision of board:
- ✔ Yes, because of Minor Mech. Corrections (no electrical issues) – no FP in Rev A!

Delay caused by:
- □ Changing requirements during design workflow
- □ Purchase or delivery problems
- □ DESY administrative delays
- □ Industrial delays
- □ Man-power problems
- □ Other reasons:
WP018 AMC/RTM (Status 05/2014)

<table>
<thead>
<tr>
<th>Module name / revision:</th>
<th>DRTM-PZT4 / 1.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modules used in WP/#r:</td>
<td>□ WP02 □ WP18, total approx. 5 pieces</td>
</tr>
<tr>
<td>Project scheduled:</td>
<td>01/2014 - 12/2014</td>
</tr>
<tr>
<td>Responsible Designer:</td>
<td>K. Przygoda</td>
</tr>
</tbody>
</table>

Module status:
- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

Module test status:
- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- High Level Software exists
- Application firmware exists

Documentation status:
- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style:
- Module was work-out in a well-defined sequence, if not why?
- A project time schedule plan exists

Current problems:
- Unclear requirements
- Unclear interfaces
- Unclear rf-power levels
- Mechanical issues
- Problems with optical sections
- Cabling or connector issues
- Internal components are not ready, which one:

- EMI PCB problems
- EMI crate problems
- Other problems:
  - lack of MMC controller for RTM, peak power consumption
  - small bugs discovered during laboratory tests (i.e. LDO en/dis)

New revision of module:
- Yes, because of
  - Design workflow
  - Purchase or delivery problems
  - DESY administrative delays
  - Industrial delays
  - Man-power problems
- Other reasons:

Actions needed to finish project:
1. Test of MMC for RTM
2. Tests of switching circuits
3. Tests of external input conditioning circuits
4. Tests of interlock circuit
5. Tests of Power amplifiers
6. Tests of external high voltage power supply
7. Inside crate tests
8. Real application tests, i.e. laser synchronization, fiber Link stabilization and cavity tuner control
WP018 FMC (Status 05/2014)

Board name / revision: DFMC-LASIO + DFMC-SFP4

Boards used in: WP18, Optical Synchronisation – 8 PCS each
Project scheduled: Q3 2014
Responsible Designer: Michael Fenner

Board status:
- ✅ Specification
- ✅ Design
- ✅ Prototype
- ✅ Debugging
- ✅ Licensing
- ✅ Pre-production
- ✅ Documentation
- ✅ Mass-production

Board tests status:
- □ Laboratory
- □ Test-stand
- □ FLASH, CMTB
- □ By manufacturer
- □ Board support package exits
- □ Application firmware exists

Documentation status:
- ✅ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- ✅ Files stored in SVN
- □ All bugs are reported in Redmine or FailureReports.docx
- □ Test procedures for production defined
- □ Internal manual exists

Working style: Board was worked-out in a well-defined sequence according to the
- □ Group board design working-plan was used,
- ✅ Guideline Design Rules were used,
- □ A project time schedule plan exists

Current problems:
- □ Unclear requirements
- □ Unclear interfaces
- □ Mechanical issues
- □ PCB is not fully assembled
- □ PCB rule violations
- □ PCB manufacturer problems
- □ PCB debugging
- □ EMI PCB problems
- □ EMI crate problems
- □ other technical problems:

Actions needed to finish project:
1. Design Finish
2. Test
3. 
4. 

New revision of board:
- □ Yes, because of

Delay caused by:
- □ Changing requirements during design workflow
- □ Purchase or delivery problems
- □ DESY administrative delays
- □ Industrial delays
- □ Man-power problems
- □ other reasons:
**Board name / revision:** DFMC-MD22 + DFMC-AD16

**Boards used in:** WP18, Optical Synchronisation – 20 PCS each

**Project scheduled:** Q3 2013

**Responsible Designer:** Robert Wedel

**Board status:**
- ☑ Specification
- ☑ Design
- ☑ Prototype
- ☑ Debugging
- ☑ Licensing
- ☑ Pre-production
- ☑ Documentation
- ☑ Mass-production

**Board tests status:**
- ☑ Laboratory
- ☑ Test-stand
- ☑ FLASH, CMTB
- ☑ By manufacturer
- ☑ Board support package exists
- ☑ Application firmware exists

**Documentation status:**
- ☑ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- ☑ Files stored in SVN
- ☑ All bugs are reported in Redmine or FailureReports.docx
- ☑ Test procedures for production defined
- ☑ Internal manual exists

**Working style:**
- Board was worked-out in a well-defined sequence according to the
- ☑ Group board design working-plan was used,
- ☑ Guideline Design Rules were used,
- ☑ A project time schedule plan exists

**Current problems:**
- ☑ Unclear requirements
- ☑ Unclear interfaces
- ☑ Mechanical Issues
- ☑ PCB is not fully assembled
- ☑ PCB rule violations
- ☑ PCB manufacturer problems
- ☑ PCB debugging
- ☑ EMI PCB problems
- ☑ EMI crate problems
- ☑ Other technical problems:

**Actions needed to finish project:**
1. Verify Rev. 2
2. 
3. 
4. 

**New revision of board:** ☑ Yes, because of

**Delay caused by:**
- ☑ Changing requirements during design workflow
- ☑ Purchase or delivery problems...
- ☑ DESY administrational delays
- ☑ Industrial delays
- ☑ Man-power problems
- ☑ Other reasons:
WP018 LDD_MEZ (Status 05/2014)

Board name / revision: LDD-10220 / 0.0

Boards used in WP/fr:

- WP02, WP18, total approx. 80 pieces

Project scheduled:

- xx/2014 - xx/2014

Responsible Designer:

Board status:

- Specification
- Design
- Prototype
- Debugging
- Licensing
- Pre-production
- Documentation
- Mass-production

Board tests status:

- Laboratory
- Test-stand
- FLASH, CMTB
- By manufacturer
- Board support package exists
- Application firmware exists

Documentation status:

- Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual)
- File structure is adapted from SVN to N group drive
- All bugs are reported in Redmine or FailureReports.docx
- Test procedures for production defined
- Internal manual exists

Working style:

- Board was work-out in a well-defined sequence according to the
d group board design working-plan was used, if not why?
- Guideline Design Rules were used, if not why?
- A project schedule plan exists

Current problems:

- Unclear requirements
- Unclear Interfaces
- Mechanical issues
- PCB is not fully assembled
- PCB rule violations
- PCB manufacturer problems
- PCB debugging
- EMI PCB problems
- EMI crate problems
- Other technical problems:

New revision of board:

- Yes, because of:
  - One mistake was corrected in old design but not in new one

Delay caused by:

- Changing requirements during design workflow
- Purchase or delivery problems
- DESY administrational delays
- Industrial delays
- Man-power problems
- Other reasons:
<table>
<thead>
<tr>
<th>Latest Board Picture</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Board Picture" /> <img src="image2.png" alt="Board Picture" /></td>
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</table>

<table>
<thead>
<tr>
<th>Board name / revision:</th>
<th>8944-01ML / 0.1</th>
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</table>

<table>
<thead>
<tr>
<th>Boards used in WP/#fr:</th>
<th>□ WP02, □ WP18, total approx. 80 pieces</th>
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</thead>
<tbody>
<tr>
<td>Project scheduled:</td>
<td>06/2012 - 08/2013</td>
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<table>
<thead>
<tr>
<th>Board status:</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ Specification, □ Design, □ Prototype, □ Debugging, □ Licensing, □ Pre-production, □ Documentation, □ Mass-production</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Board tests status:</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ Laboratory, □ Test-stand, □ FLASH, □ CMTB, □ By manufacturer</td>
</tr>
<tr>
<td>□ Board support package exists, □ Application firmware exists</td>
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</tbody>
</table>

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<tr>
<th>Documentation status:</th>
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<td>□ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User- Manual)</td>
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<td>□ Internal manual exists</td>
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<th>Working style:</th>
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<tbody>
<tr>
<td>Board was work-out in a well-defined sequence according to the</td>
</tr>
<tr>
<td>□ Group board design working-plan was used, if not why?</td>
</tr>
<tr>
<td>□ Guideline Design Rules were used, if not why?</td>
</tr>
<tr>
<td>□ A project time schedule plan exists</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current problems:</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ Unclear requirements, □ Unclear interfaces</td>
</tr>
<tr>
<td>□ Mechanical issues, □ PCB is not fully assembled</td>
</tr>
<tr>
<td>□ PCB rule violations, □ PCB manufacturer problems, □ PCB debugging</td>
</tr>
<tr>
<td>□ EMI PCB problems, □ EMI crate problems</td>
</tr>
<tr>
<td>□ other technical problems:</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Actions needed to finish project:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
</tr>
<tr>
<td>2.</td>
</tr>
<tr>
<td>3.</td>
</tr>
<tr>
<td>4.</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>New revision of board:</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ Yes, because of</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Delay caused by:</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ Changing requirements during design workflow</td>
</tr>
<tr>
<td>□ Purchase or delivery problems, □ DESY administrative delays, □ Industrial delays</td>
</tr>
<tr>
<td>□ Man-power problems</td>
</tr>
<tr>
<td>□ other reasons:</td>
</tr>
</tbody>
</table>
### WP018 LDD_MB2 (Status 05/2014)

<table>
<thead>
<tr>
<th>Board name / revision:</th>
<th>10386 / 0.0</th>
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</thead>
<tbody>
<tr>
<td>Boards used in WP/#:</td>
<td>□ WP02, □ WP18, total approx. 10 pieces</td>
</tr>
<tr>
<td>Project scheduled:</td>
<td>01/2014 - 09/2014</td>
</tr>
<tr>
<td>Responsible Designer:</td>
<td></td>
</tr>
<tr>
<td>Board status:</td>
<td>□ Specification, □ Design, □ Prototype, □ Debugging, □ Licensing, □ Pre-production, □ Documentation, □ Mass-production</td>
</tr>
<tr>
<td>Board tests status:</td>
<td>□ Laboratory, □ Test-stand, □ FLASH, CMTB, □ By manufacturer, □ Board support package exits, □ Application firmware exists, □ Internal manual exists</td>
</tr>
<tr>
<td>Documentation status:</td>
<td>□ Production files are generated (FP, STEP, Gerber, Assembly, Layer-stack, Datasheet, User-Manual), □ File structure is adapted from SVN to N group drive, □ All bugs are reported in Redmine or FailureReports.docx, □ Test procedures for production defined, □ Internal manual exists</td>
</tr>
<tr>
<td>Working style:</td>
<td>Board was work-out in a well-defined sequence according to the plan, □ Group board design working-plan was used, □ Guideline Design Rules were used, □ A project time schedule plan exists</td>
</tr>
<tr>
<td>Current problems:</td>
<td>□ Unclear requirements, □ Unclear interfaces, □ Mechanical issues, □ PCB is not fully assembled, □ PCB rule violations, □ PCB manufacturer problems, □ PCB debugging, □ EMI PCB problems, □ EMI crate problems, □ other technical problems:</td>
</tr>
<tr>
<td>Actions needed to finish project:</td>
<td>1. Mass-production of the corrected PCBs, 2. Assembling of PCBs, 3.</td>
</tr>
<tr>
<td>New revision of board:</td>
<td>□ Yes, because of</td>
</tr>
<tr>
<td>Delay caused by:</td>
<td>□ Changing requirements during design workflow, □ Purchase or delivery problems, □ DESY administrational delays, □ Industrial delays, □ Man-power problems, □ other reasons:</td>
</tr>
</tbody>
</table>

Two capacitors should be changed to another type.
Conclusions for HW development (05/2014)

Management problems:
- Insufficient specification caused by not detailed high level system planning
- Last-minute requirements change
- No consequent bug/failure tracking
- Missing Board reviews (we are changing this)

Lack of time:
- 19” module development and finishing needs more resources
- Too many projects simultaneously
- Top down working plan and guidelines are ignored
- Missing documentation
- No clear fabrication information
- Mechanics not checked carefully enough

Bad habits:
- Too many Library Sources
- PCB and Schematic checks are partially ignored
WP02 / WP18 Hardware Statistics (05/2014)

WP02 (statistics)

Delay caused by:
- 10 of 16 marked: “Changing requirements during design flow”
- 09 of 16 marked: “Man-power problems”

Documentation status:
- 6 of 16 did no failure in entry Redmine or FailureReport.docx

Working Style:
- 10 of 16 did not follow the PCB working plan or PCB guidelines
- 03 of 16 used the PCB working plan
- 03 of 16 used the PCB guidelines

WP18 (statistics)

Delay caused by:
- 00 of 8 marked: “Changing requirements during design flow”
- 00 of 8 marked: “Man-power problems”

Documentation status:
- 6 of 8 did no failure entry in Redmine or FailureReport.docx

Working Style:
- 05 of 8 did not follow the PCB working plan or PCB guidelines
- 00 of 8 used the PCB working plan
- 03 of 8 used the PCB guidelines

Thanks for your attention!