Hardware for LLRF Control System in MTCA Standards

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Introduction

LLRF control systems of modern linear accelerators require acquisition of data from hundreds of analogue channels with sampling rates of around 100 MHz and real-time signal processing within a few hundred nanoseconds. The LLRF control system of FLASH accelerator was designed using µTCA (micro-Telecommunications Computing Architecture) standard. The prototype system is based on draft of the MTCA.4 specification developed by PICMG organisation. The LLRF control system hardware is composed of several data acquisition cards, timing module, data processing module and vector modulator. The data processing module, the µTCA-based Controller (µTC), was designed as a double-width Advanced Mezzanine Card (AMC) that cooperates with vector modulator (µVM) realised as a micro-Rear Transition Module (µRTM).

µTC - µVM Cooperation

The board should be designed as a double-width, AMC module according to PICMG MTCA.4 draft
µTC shall provide enough computation power for cavity field and fast beam-based feedback controllers
µTC should provide non-volatile memory for FPGA, embedded soft processor and DSP
µTC shall provide fast volatile memories for data buffering
The configuration and control shall be performed using the PCIe interface on the µTCA backplane
Low-latency gigabit connections shall be available on the backplane and on the front-panel as an optical links with latency less than 200 ns
Module Management Controller (MMC) providing base IPMI functionality and a firmware upgrade feature
The controller shall cooperate with a module of Vector Modulator designed as a µRTM, provide communication links, power supply and management functionality

The Hardware Solution

Computation power:
- Virtex-5 XC5VSX95T FPGA device and floating point Tiger Sharc TS-201 DSP processor
- FPGA provides high-speed serial transceivers, soft processor and data processing logic
- Quad-Data Rate (QDR-II) and Double-Data Rate (DDR2) memories

Communication links:
- FPGA provides serial links, using embedded GTP transceivers:
  - Low-latency gigabit communication (backplane and front-panel)
  - PCI Express x4
  - Gigabit Ethernet

Intelligent Platform Management Controller:
- Module Management Controller (MMC) required by AMC specification
- Based on ATMEGA1281 microcontroller and CPLD circuit
- Platforms communication with the supervising system and handling commands compatible with IPMI specification
- MMC with µRTM module management compatible with xTCA for Physics specification
- In-system firmware upgrade of FPGA and DSP

Laboratory Tests

The µTC hardware was tested in the laboratory at the Department of Microelectronics and Computer Science and in the Deutsches Elektronen-Synchrotron (DESY) research facility.

The picture presents two µTC boards installed in 12-slot µTCA shelf during tests at DESY.

The µTC-based Controller board is one of only a few devices that were designed with accordance to the draft of the MTCA.4 specification. The µTC provides considerable processing power, large number of high-throughput serial links and flexible configuration schemes. This, combined with a high reliability and serviceability renders the µTC an universal platform, well suited for implementation of accelerator control equipment.

The board operation was successfully verified during the tests of the LLRF control system of the FLASH accelerator in July and August 2011.

Summary

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