Development of Control System for Fast Frequency Tuners of Superconducting Resonant Cavities for FLASH and XFEL Experiments

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Development of Control System for Fast Frequency Tuners of Superconducting Resonant Cavities for FLASH and XFEL Experiments

by

Konrad Przygoda

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Łódź, 2010
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<th>Meaning</th>
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<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>AMC</td>
<td>Advanced Mezzanine Card</td>
</tr>
<tr>
<td>ATCA</td>
<td>Advanced Telecommunications Computing Architecture</td>
</tr>
<tr>
<td>CAMAC</td>
<td>Computer Automated Measurement And Control</td>
</tr>
<tr>
<td>COORDIC</td>
<td>COordinate Rotation Digital Computer</td>
</tr>
<tr>
<td>CuBe</td>
<td>Copper-beryllium</td>
</tr>
<tr>
<td>CW</td>
<td>Continues Wave</td>
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<tr>
<td>DAQ</td>
<td>Data Acquisition</td>
</tr>
<tr>
<td>DESY</td>
<td>Deutsches Elektronen-Synchrotron</td>
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<tr>
<td>DMCS</td>
<td>Department of Microelectronics and Computer Science</td>
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<tr>
<td>DOOCS</td>
<td>Distributed Object Oriented Control System</td>
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<tr>
<td>EM</td>
<td>Electromagnetic</td>
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<tr>
<td>FEL</td>
<td>Free Electron Laser</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
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<tr>
<td>FLASH</td>
<td>Free Electron Laser in Hamburg</td>
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<tr>
<td>FNAL</td>
<td>Fermi National Lab</td>
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<tr>
<td>HOM</td>
<td>Higher Order Mode</td>
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<tr>
<td>HTS</td>
<td>Horizontal Test Stand</td>
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<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
</tr>
<tr>
<td>ILC</td>
<td>International Linear Collider</td>
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<tr>
<td>IPMC</td>
<td>Intelligent Platform Management Controller</td>
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<tr>
<td>LFD</td>
<td>Lorentz Force Detuning</td>
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<tr>
<td>LINAC</td>
<td>Linear accelerator</td>
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<tr>
<td>LLRF</td>
<td>Low-Level Radio Frequency</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
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<tr>
<td>MCP</td>
<td>Mirco-channel Plate</td>
</tr>
<tr>
<td>MFC</td>
<td>Multichannel Field Controller</td>
</tr>
<tr>
<td>MMC</td>
<td>Module Management Controller</td>
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<tr>
<td>MO</td>
<td>Master Oscillator</td>
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## Development of Control System for Fast Frequency Tuners of Superconducting Resonant Cavities for FLASH and XFEL Experiments

<table>
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<th>Acronym</th>
<th>Description</th>
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<td>MTS</td>
<td>Module Test Stand</td>
</tr>
<tr>
<td>NIM</td>
<td>Nuclear Instrumentation Module</td>
</tr>
<tr>
<td>NML</td>
<td>New Muon Lab</td>
</tr>
<tr>
<td>PCIe</td>
<td>Peripheral Component Interconnect Express</td>
</tr>
<tr>
<td>PI</td>
<td>Piezo Instrumente</td>
</tr>
<tr>
<td>PZD</td>
<td>Piezo Driver</td>
</tr>
<tr>
<td>PZT</td>
<td>Piezoelectric Transducer</td>
</tr>
<tr>
<td>R&amp;D</td>
<td>Research and Development</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RMC</td>
<td>Module Management Controller</td>
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<tr>
<td>RTM</td>
<td>Rear Transition Module</td>
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<tr>
<td>SASE</td>
<td>Self Amplified Spontaneous Emission</td>
</tr>
<tr>
<td>SC</td>
<td>Superconducting</td>
</tr>
<tr>
<td>SCRS</td>
<td>Superconducting Resonant</td>
</tr>
<tr>
<td>SerDes</td>
<td>Serializer/Deserializer</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SRT</td>
<td>Sweeney, Robertson, Tocher</td>
</tr>
<tr>
<td>TESLA</td>
<td>Tera-eV Superconducting Linear Accelerator</td>
</tr>
<tr>
<td>TM010</td>
<td>Fundamental accelerating mode</td>
</tr>
<tr>
<td>TNC</td>
<td>Industrial standard connector</td>
</tr>
<tr>
<td>TTF</td>
<td>TESLA Test Stand</td>
</tr>
<tr>
<td>TUL</td>
<td>Technical University of Lodz</td>
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<tr>
<td>UV</td>
<td>Ultraviolet</td>
</tr>
<tr>
<td>VME</td>
<td>Versa Module Eurocard</td>
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<tr>
<td>VXI</td>
<td>VME eXtensions for Instrumentation</td>
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<tr>
<td>XFEL</td>
<td>X-Ray Free Electron Laser</td>
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<td>µTCA</td>
<td>micro TCA</td>
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1. INTRODUCTION

The main objective for the Free Electron Lasers (FELs) is to generate X-ray flashes. With the use of X-rays, scientists will be able to map the atomic details of viruses, decipher the molecular composition of cells, and take three-dimensional images of the nanoworld. The X-radiation will also enable scientists to film chemical reactions and study processes that occur deep inside planets.

In order to generate X-ray flashes, bunches of electrons must be at first accelerated to high energies and then directed through special arrangements of magnets (undulators). In the process, the particles will emit radiation that is amplified increasingly until an extremely short and intense X-ray flash is finally generated.

The superconducting resonant cavities are used for accelerating electrons to high energies. The cavity resonators contain niobium metal. If niobium is cooled down to approximately 9.5 K, it becomes superconducting [1]. This means that it loses its electric resistance and conducts currents with very low loses. As a result, all of the energy fed into the cavities can be transferred to electrons. The linear accelerators, which are used to power the FEL machines, are composed primarily of superconducting cavities [2].

At present, there are many laboratories and FEL machines in operation and several are planned to begin operation in the near future [3][4][5]. One of the most promising machines is the Free Electron Laser in Hamburg (FLASH) [5]. FLASH accelerator can generate radiation from ultraviolet (UV) to soft X-ray range and it is the pilot facility for a bigger machine known as the European X-Ray Free Electron Laser (XFEL) [6]. The XFEL is projected to be completed in 2013.

The FLASH accelerator is operated in pulse mode with repetition rate up to 10 Hz. The typical time duration of a radio frequency (RF) pulse is about 2 ms. The electromagnetic wave, transmitted to the cavity as a set of successive pulses, causes strong mechanical stresses inside the cavity. The mechanical deformations of thin cavity walls are typically caused by repulsive magnetic forces as well as attractive electric forces, mainly due to the Lorentz forces. The cavity is very susceptible to small changes in dimension because of a very narrow RF resonance bandwidth, in the order of 300 Hz and a high quality factor, in the order of $10^6$. Even a micrometer variation per one meter of resonator dimension can
cause the cavity detuning from its resonant frequency by several hundred Hz. The detuned cavity reflects more input power, and as a result, it needs more RF control effort to achieve desired FEL conditions.

The cavity can be tuned to a resonance frequency using slow and fast frequency tuners. The slow frequency tuners are based on step motors which can tune the cavity within a range of a few hundred kHz. Nevertheless, the time response of such elements is quite limited and equals to even a single minute. Therefore, the fast frequency tuners, commonly based on piezoelectric materials, are used for active compensation of cavity detuning during the RF pulse.

The piezo elements, considered as a capacitive load (~5 µF), need very sophisticated driving circuits. The voltage range that can be applied to piezo tuners is also limited to several tens of volts. Furthermore, the sharp current transitions of applied driving signal can decrease significantly the lifetime of piezostacks. A very stable, high-current efficient power supply of the driving circuit can also play a crucial role in controlling piezoelectric elements. Since the FLASH accelerator has only 40 cavities (equipped with both single and double piezo tuners) and the XFEL will use around 800 cavities (with double piezos packed into 100 accelerating modules), a distributed architecture with multichannel digital and analog control circuits seems to be essential [6].

Although, the theoretical aspects of piezo control were already studied and well understood, especially in [7][8][9][10], there are still many questions to be answered, for example related to hardware implementation. The most sought-after issue is high-voltage, high-current piezo driving circuit dedicated to multi-cavity configuration. The automation of piezo tuners control and its multi-cavity demonstration are also a real challenge, especially for high accelerating field gradient operations [11][12][13][14][15]. Since the piezo compensation system should fulfill the main requirements for FEL operation, (especially for high-gradient, high-current experiments), its permanent installation and commissioning are strongly recommended.
The key issue of this thesis is to present the recent development of the control system for fast frequency tuners of superconducting resonant cavities assembled for linear accelerators such as the FLASH or XFEL. This dissertation especially focuses on proving that:

1. **it is possible to perform a simultaneous Lorentz force detuning compensation for each superconducting resonant (SCRS) cavity over a single accelerating module using a carefully-designed driving circuit of fast frequency tuners based on piezoelectric elements,**

2. **it is possible to reduce detuning of superconducting (SC) cavity from an electrical resonance frequency of 1.3 GHz to less than 10 Hz for high accelerating field gradient operations of the order of 30 MV/m,**

3. **it is possible to assess the effectiveness of the Lorentz force detuning compensation system using measurements of forward power (transmitted to the cavity), reflected power (reflected from the cavity) as well as cavity power (stored inside the cavity).**

This dissertation is organized into seven chapters. The first chapter introduces the major accelerator technologies used for FEL machines with special emphasis on the FLASH accelerator. The chapter also shows the main problems that need to be solved when using the control systems for the fast frequency tuners.

The second chapter provides information about the FLASH and the XFEL linear accelerators with special attention paid to its achievable parameters. Moreover, the main accelerating field errors as well as Low-Level Radio Frequency (LLRF) control systems used for their control are summarized briefly. Finally, there is a short summary of the background of previously installed fast frequency tuners control systems for the FLASH facility.

The third chapter presents the fast frequency tuners used for resonance frequency control of SC cavities. Furthermore, details on prototype design of the high-voltage, high-current driving circuit for these elements and its FLASH demonstration for 8 superconducting cavities are presented.

The fourth chapter shows the main requirements for the control system of the fast frequency tuners with their typical control scheme. Moreover, the main parts of the developed control algorithms are derived and summarized. A special emphasis are put on
the cavity detuning computation algorithm, as it is the most important input for the developed digital controller.

The fifth chapter introduces the piezo control system installed in the FLASH facility. Moreover, it gives a report about the high energy physics experiments carried out in the FLASH with piezo compensation support. The main results obtained during high-gradient, high-current beam acceleration tests are discussed. The chapter concludes with the measurements of piezo compensation system effectiveness.

The sixth chapter presents the concept of the migration of the existing piezo control system to Advanced Telecommunication Computing Architectures (ATCA), which are expected to be used in the XFEL experiment.

The seventh chapter summarizes the dissertation and gives a short outlook for the future plans.

The dissertation has 4 appendices. Appendix A: presents a short report on piezo measurements of gradient versus piezo pulse amplitude for both maximum as well as nominal operating conditions of accelerating module ACC6. Appendix B: gives an explanation of attenuation of cavity mechanical vibrations. Appendix C: discusses the crosstalk measurements referring to the driving circuit as well as the driven object. In this case, the driven object is an accelerating module composed of 8 SC cavities equipped with fast frequency tuners. Appendix D: gives the technical documentation for the designed hardware PCBs.
2. MAIN FACILITY RESEARCH

The Free Electron Laser in Hamburg was the main facility research for this thesis. The FLASH laser is driven by superconducting linear accelerator (LINAC). The main parts of the linac machine are TESLA\(^1\) superconducting resonant cavities. The Low-Level Radio Frequency control system is commonly used for controlling an accelerating field inside the SC cavities as well as for stabilizing its main disturbances. This paragraph explains a principle of FEL machine operation, describes the most frequent accelerating field errors and their impact on the modulation of cavity resonance frequency. What is more, there are described briefly the main LLRF control system of FLASH and short background to the control of the fast frequency tuners.

2.1. FLASH Overview

The FLASH laser is situated in Deutsches Elektronen-Synchrotron (DESY) research center in Hamburg, Germany \([5]\). The main part of FEL machine is the RF linac where the particles move along a straight tube. The particles pass through a linac only once, unlike the particles in cyclotron or synchrotron ring-shaped accelerators that make many revolutions, gaining energy each time. The RF linac accelerates an electron beam to high relativistic energies. High energy beam is passed through undulator where the beam is converted to photon stream. The FLASH laser offers many desirable characteristics, that comparing to conventional lasers, are desirable i.e. wavelength tuning, high average power and high efficiency of converting an electric to laser power. Because the lasing principle does not involve transitions between the fixed atomic or molecular levels, as in chemical lasers, wavelength of the Free Electron Laser in Hamburg is tuned by adjusting the desired beam energy. The FLASH facility is mainly used for experiments with short-wavelength UV and soft X-rays radiation of order of tens nm. The block diagram of the FLASH facility is shown in Fig. 2.1.

\(^{1}\) TESLA – Tera-eV Superconducting Linear Accelerator \([2]\)
2.1.1. Laser and RF Gun

The source of particles at FLASH is a photo injector, where electrons are generated by means of the photo effect. The laser is based on the cathode of cesium telluride, where electrons are liberated with a periodicity of 1 μs and total length of 800 bunches. The cathode is supported by 1.5 cell L-band copper resonator which provides an accelerating field directly at the origin of particle production of 5 MeV. The resonator of the RF photo injector is often referred to as the RF Gun. Particles, when they passed through RF Gun, are further accelerated downstream the SC linac to the required energy of FEL operation of about 1 GeV.

2.1.2. SC Linac

A key component of SC linac is a device that imparts energy to the charged particles. This is an electromagnetic cavity resonating at a microwave frequency. The TESLA SCRS cavity is a 9-cell standing wave structure of about 1 m long, which fundamental accelerating mode (TM010) resonates at 1.3 GHz. The cavity is made of solid niobium and it is cooled by super fluid helium at 2 K. It operates in such a low temperature because niobium material becomes a superconductor below 9 K, what means the whole beam current is transferred to the beam energy due to the fact that cavity resistance can be neglected in such conditions. Each 9-cell cavity is equipped with stiffening rings (see section 2.3), titanium helium tank, a tuning system driven by a stepping motor (slow tuner) and so-called piezo translator (fast tuner), a coaxial RF power coupler capable of transmitting more than 200 kW, a pickup probe and two higher-order mode (HOM) couplers, as seen in Fig. 2.2. To reduce the cost of cryogenic installations, eight TESLA cavities are mounted in a common vacuum vessel and constitute so-called cryomodule (accelerating structure) of the RF linac. The FLASH machine consists of 6 cryomodules grouped into three RF stations – ACC1, ACC2/3 and ACC4/5/6 (see Fig. 2.1). Each RF station assures desired RF power for high-current beam acceleration. The peak current of
the uncompressed bunch is about 70 A. In order to achieve a peak current exceeding 2 kA (required for FEL operation), a compression of the bunch using magnetic chicanes (bunch compressors) is done in two steps at energies of 130 MeV and 470 MeV. The achievable electron beam energy in such configuration can reach up to 1 GeV. Each RF station is powered by 10 MW klystron. The single high power RF generator is capable of driving up to 4 accelerating modules (instead of using many low power generators) with the RF pulses of electromagnetic wave frequency of 1.3 GHz. The typical RF pulse duration is about 2 ms with maximum repetition rate of 10 Hz (klystron limitation).

Fig. 2.2. Superconducting 1.3 GHz 9-cell TESLA cavity used for FLASH facility – cavity picture (top) and schematic drawing (bottom) [1].

2.1.3. Undulator

Single-pass high gain FELs require a long undulator system. The FLASH undulator system consists of six modules, each is 4.5 m long. The fixed gap is 12 mm long with a peak magnetic field of 0.48 T, realized with permanent NdFeB magnets. The undulator consists of a periodic structure of dipole magnets with a total length of 27.3 mm. A pair of electromagnetic superconducting quadrupoles among each of six modules provides a large acceptance in beam energy. In terms of FEL radiation it covers the wavelength range from 120 to 5 nm.
The principle of FEL operation is based on SASE\(^2\) effect. This process amplifies spontaneous undulator radiation generated by stochastic noise in the high energy electron bunch. In long undulator sections, due to interaction with the alternating magnetic field, the electrons are redistributed to so-called micro-bunches which can radiate coherently as a brilliant stream of photons (see Fig. 2.3).

### 2.1.4. FEL Diagnostics

The FEL diagnostics are mainly used for determining online the important photon beam parameters, such as intensity, spectral distribution and temporal structure. An important instrument for tuning the onset of laser amplification and optimizing the lasing is a detector based on gold wires and a micro-channel plate (MCP). The dynamic range of the detector is sufficient to cover several orders of radiation energy magnitude, from spontaneous (~7 nJ) to the amplified emission (50 ÷ 100 µJ). The detector has been carefully calibrated and its relative accuracy is in the order of 1%. The radiation energy has been cross-calibrated with the gas monitor detectors to meet an absolute measurement uncertainty of 25%. View screens using Ce:YAG crystals are situated at various locations. A dedicated monochromator device is used for measuring a single shot spectra. It is equipped with the intensified CCD camera and has a resolution of 0.02 nm and the absolute calibration error below 0.03 nm [5].

The new accelerating modules of ACC1, ACC7 and 3\(^{rd}\) harmonic ACC39 have been installed after the FLASH upgrade that took place during 2009/2010 shutdown. The

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\(^2\) SASE – Self Amplified Spontaneous Emission
Development of Control System for Fast Frequency Tuners of Superconducting Resonant Cavities for FLASH and XFEL Experiments

Present beam and FEL performance of the FLASH accelerator are briefly summarized in Tab. 2.1.

Tab. 2.1 FLASH accelerator parameters.

<table>
<thead>
<tr>
<th>Main parameters</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Length</td>
<td>m</td>
<td>&gt;300</td>
</tr>
<tr>
<td>No. RF stations</td>
<td>unit</td>
<td>5</td>
</tr>
<tr>
<td>No. accelerating modules</td>
<td>unit</td>
<td>8</td>
</tr>
<tr>
<td>RF Klystrons</td>
<td>MW</td>
<td>5</td>
</tr>
<tr>
<td>1\textsuperscript{st} / 3\textsuperscript{rd} harmonic cavities</td>
<td>unit</td>
<td>56 / 4</td>
</tr>
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<table>
<thead>
<tr>
<th>Electron beam</th>
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<tbody>
<tr>
<td>Typical accelerating field gradient</td>
<td>MeV/m</td>
<td>&gt; 25</td>
</tr>
<tr>
<td>Typical bunch train length</td>
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<td>800</td>
</tr>
<tr>
<td>RF pulse repetition rate</td>
<td>Hz</td>
<td>max. 10</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FEL operation</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavelength</td>
<td>nm</td>
<td>47-6.5</td>
</tr>
<tr>
<td>Energy</td>
<td>GeV</td>
<td>1.2</td>
</tr>
</tbody>
</table>

2.2. European XFEL

The FLASH accelerator is also called a prototype for a new project called European XFEL [6]. The XFEL large scale machine will produce coherent radiation of X-Rays range which will allow for penetrating currently unknown places of matter, i.e. Higgs bosons, black matter and other micro cosmos. The FEL machine will consist of RF Gun, superconducting linac as well as long sections of undulators and other FEL diagnostics. The total beam energy generation of (20 ÷ 50) GeV, required for X-Rays, will be achievable using about 800 accelerating modules packed into 25 RF stations of the main linac. The long undulator sections will support the SASE process of tuning wavelength from 6 nm up to less than 0.1 nm. It was decided to situate the XFEL facility in DESY in Hamburg and at the initial stage its length will exceed 3 km. The block diagram of the XFEL machine is shown in Fig. 2.4. The main parameters proposed for XFEL machine are shown in Tab. 2.2.
Since the FLASH accelerator with its 8 cryomodules operates using a Versa Module Eurocard (VME) standard digital and analog control systems, more sophisticated hardware as well as software architectures need to be improved to meet the configuration of such large scale machine as the XFEL facility. The Advanced Telecommunications Computing Architecture, with its modular design, hot-swapping, redundancy for the most crucial circuits as well as power bus for single relatively high-voltage is proposed to build LLRF control system for XFEL. The last chapter of the thesis presents the concept of integrating piezo compensation system with ATCA standards. Moreover, first results of the prototype system tests will be shown.
2.3. **Accelerating Field Errors**

Energy fluctuations of the accelerated electron beam along SC linac are caused by various phenomena. The mostly frequent errors are described in the following sections.

2.3.1. **Microphonics**

Mechanical vibrations caused by the accelerator environment are always present and may be transferred to the accelerating structures via many different sources [16][20]. The beam tubes can transfer to the cavities the vibrations caused by vacuum pumps. Man-made noise (traffic, machinery) or only ground motions (seismic activities, ocean waves or elastic motion produced by the moon) are imposed on the linear accelerator through the ground and the supports. *One of the major microphonics can also be induced by the piezo compensation itself when it is performed with high repetition rates up to tens of Hz of the RF field pulse.* The microphonics vibrations can modulate the cavity resonance frequency within a range of tens Hz, as seen in Fig. 2.5. The microphonics errors can play a significant role in continuous wave (CW) operated linacs. The CW operated linacs use SC cavities with bandwidth of tens Hz. As a result, the microphonics noise lower than 10 Hz can detune significantly such structure and makes the beam unstable. To improve the beam stability for CW operation, the first method for its identifying as well as compensating has been presented briefly in [20].
For the pulse operated linacs, microphonic vibrations modulate resonance frequency only from pulse to pulse, but not during the RF pulse and as a consequence, they are not so crucial for beam acceleration, as seen in Fig. 2.6. In spite of the fact, the microphonic noise can generate the unexpected energy fluctuations, i.e. for SASE tuning experiments and therefore the methods for its identification as well as cancellation should be considered (see Appendix B:).

2.3.2. The Lorentz force detuning

The TESLA cavities are operated with high quality factors of order of $3 \times 10^6$ what results in bandwidth of the accelerating structure of order of 300 Hz. Compared to the main resonance frequency of 1.3 GHz, this indicates the high sensitivity of SC cavities to strong
mechanical stresses. The mechanical stresses are commonly induced by the electromagnetic field surrounding thin cavity walls. As a result, the electromagnetic field exerts the Lorentz force on the current induced in a thin surface layer of the cavity resonator. The resulting pressure acting on the cavity wall is

\[ p = \frac{1}{4} (\mu_0 H^2 - \varepsilon_0 E^2) \tag{2.1} \]

where \( \mu_0, \varepsilon_0 \) mean permittivity and permeability of free space and \( H, E \) mean electric and magnetic fields intensity.

This pressure leads to a deformation of cells in \( \mu \text{m} \) range and a change \( \Delta V \) in their volume. The consequence is a frequency shift \( \Delta f \) of order of hundred Hz according to Slater’s rule

\[ \frac{\Delta f}{f_0} = \frac{1}{4W} \int_{\Delta V} (\varepsilon_0 E^2 - \mu_0 H^2) dV \tag{2.2} \]

where

\[ W = \frac{1}{4} \int_V (\varepsilon_0 E^2 - \mu_0 H^2) dV \tag{2.3} \]

is the stored energy and \( f_0 \) is resonant frequency of the unperturbed cavity. It was experimentally proved that the frequency shift at 25 MV/m is close to 900 Hz for the unstiffened cavity with 2.5 mm thick wall. In order to reduce the phenomena, the special stiffening rings are welded between adjacent cells in the cavity as shown in Fig. 2.7. They reduce the frequency shift to about 500 Hz for 1.3 ms long RF pulse operated with accelerating field gradient of more than 20 MV/m. The deformation of the stiffened cell is negligible near the iris, where the electric field is large, but remains nearly the same as in the unstiffened cell near the equator, where the magnetic field dominates (see Fig. 2.7). The deformation in this region can be reduced only by increasing the wall thickness [1].
Although, it is possible to increase the wall thickness to enhance cavity rigidity, the cavity walls should be kept as thin as possible to ensure more effective cooling and reduce material costs. As a compromise, the wall thickness of the TESLA cavities has been chosen to be 2.8 mm. The Lorentz force detuning is a gradient dependent and under steady-state conditions, concerning the flat top duration of the RF field pulse, it is proportional to the square of the accelerating field gradient (see Fig. 2.8 top right). It is clearly visible that cavity detuning becomes substantial above 25 MV/m.
Fig. 2.8. Measurements of Lorentz force detuning (to left) for different accelerating field gradients (RF pulse flat top duration ~800 µs) and linear fitting curve of flat top duration detuning (top right). RF control effort measurements for different resonance frequency shifts in cavity (bottom) at nominal operating conditions [21].

Maintaining constant accelerating field in detuned structure requires an extra RF power, mainly due to increased reflection ratio. It was proved that the RF control efforts (klystron power per cavity) can be increased to 25% in the Lorentz force detuned cavities when operating with high accelerating field gradients above 25 MV/m, as seen in Fig. 2.8 bottom.

2.4. LLRF Control

The LLRF control system stabilizes the amplitude (0.03%) and phase (0.03 deg.) of electromagnetic (EM) field inside the SC cavities. Therefore, it is essential for stable and reliable beam acceleration [22]. The most basic function of LLRF control system is a fast feedback loop that measures a vector sum of individual cavities accelerating fields and attempts to hold it at the desired set-point value. The amplitude and phase control of the cavity accelerating field is achieved by modulating the signal driving the klystron (upconversion) through a vector modulator device. The cavity RF signal is downconverted
to an intermediate frequency (IF), while preserving the amplitude and phase information. A digital stage performs the needed feedback algorithm. The ADC and DAC converters link the analog and digital parts of the control system [23][24][25][26][27]. The configuration and management of the system as well as visualization of measurements are performed using fast Ethernet interface and dedicated client-server applications – DOOCS servers [28]. The block diagram of the RF system architecture of FLASH with LLRF control is shown in Fig. 2.9.

As it was already mentioned, the detuned cavities need more RF control efforts to achieved desired FEL operation conditions. The fast frequency tuners based on piezo translators are commonly used for active compensation of the Lorentz force detuning effect for pulsed operated cavities. Since the fast piezo tuners need a very sophisticated control circuit, the main part of its control is dedicated to power amplifiers – piezo drivers. The piezo drivers are driven with small voltage signals using DAC converters. Since the piezos can also operate also as sensors, they are connected to ADC converters.

**Fig. 2.9.** The block diagram of the RF system architecture of FLASH [29]. The RF station is driven with single klystron. The digital feedback system is applied for accelerating field control. The RF system is synchronized using master oscillator reference. The LLRF control is triggered using dedicated timing blocks.

DOOCS – Distributed Object Oriented Control System

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2.5. Motivation

The first control of fast frequency tuners at DESY was demonstrated in [21]. As a proof of the experiment the Lorentz force detuning compensation for a single cavity equipped with the fast frequency tuner based on single piezo element was achieved by using compensation signal tuned manually. The experiment was performed with the use of commercially designed single channel power amplifier driven by the external laboratory function generator. The first automatic control of the Lorentz force detuning for a single cavity equipped with the fast frequency tuner was demonstrated by Przemysław Sękalski from Department of Microelectronics and Computer Science (DMCS) at Technical University of Łódź (TUL) and briefly described in [10]. The proposed piezo control system was based on 2-channel piezo driver unit (developed by DESY) driven by LLRF DAC board and it was used mainly for research and development (R&D) activities. Even a simple closed loop operation of the proposed solution was demonstrated, the controller response was a few times of the repetition rate of the RF field pulse. As a result, the fast feedforward operation between each RF pulse was not possible even for a single cavity. Since, the FLASH accelerator was planned to be equipped with 5 accelerating modules, each comprising of 8 superconducting cavities, the applied control system was not acceptable for permanent installation. The performance of the Lorentz force detuning compensation was also demonstrated in [12]. The proposed piezo control system was installed temporarily for Module Test Stand (MTS) facility and used for the fast frequency tuners characterization of the SC cavities operated with high accelerating field gradients. The control system of piezo tuners, described in [10], was exchanged for Simcon 3.1 LLRF control board used for generating compensation signals with the use of the FPGA device and fast DAC converters. Since, the maximum range of output voltage of the DAC converters ported to the Simcon 3.1 board was ±1 V and the maximum gain of 2-channel piezo driver unit was 40 V/V, it was not possible to use such system for the Lorentz force detuning compensation when cavities were operated with high accelerating field gradients. As a result, further activities concerning multi-cavity configuration were performed by using 2 external laboratory function generators split into 4 units that consists of 2-channel piezo driver units. As one can notice, all the proposed solutions were not so efficient and they needed further hardware, firmware as well as control software developments. The high-voltage, high-current driving circuits suitable for multi-cavity configuration are the
most coveted. The automation of piezo tuners control and its multi-cavity demonstration are also real challenge and as a proof of experiment it becomes primary purpose of the controller development. Since, the piezo compensation system should meet the main requirements demand for FEL operation, especially for high-gradient, high-current experiments, its development and permanent installation for the FLASH facility becomes the target issue of the dissertation.
3. PIEZO TUNERS CONTROL

The piezo tuners are essential for controlling frequency of cavity resonance, especially when it operates in pulse mode with high accelerating field gradients. The piezo tuners are the integral parts of cavity mechanical tuners, and for TTF\textsuperscript{4} tuner design, they are assembled on the edge of each cavity along the cryomodule. The fast frequency tuners should be controlled by sophisticated driving circuits. The driving circuit should be designed in a way allowing for the simultaneous Lorentz force detuning compensation of 8 cavities along the single accelerating module. This paragraph introduces the fast frequency tuners and the driving circuits used for controlling them. Since the driving circuit is the most critical part of the piezo compensation system, its main parameters are discussed briefly. Finally, the tests carried out on the designed driving circuits in real accelerator environment are shown.

3.1. Frequency Tuners

The cavity resonance frequency should be kept close to the resonance range as long as possible, especially at the time when the electron beam is accelerated. To achieve this goal, the special mechatronic devices, frequency tuners, are applied [30]. The usual tuning method for superconducting cavities is to change the cell length by adjusting mechanically the overall length of the cavity. Since all the cavity cells are very similar mechanically, each cell changes by the same amount that means the overall field profile is not affected. A consideration with respect to the extent of the tuning range is the elastic limit of niobium material. Keeping the elastic limit gives a tuning range of several hundred kHz. Currently, there are two main structures of such devices which are under development for superconducting cavities. The first solution, named as TTF tuner (Saclay tuner I and II), is accomplished by a mechanical device that modifies the cavity length driven by a stepper motor unit. The leverage system is designed in order to reduce stresses on the stepper motor and to enhance enough sensitivity. The stepper motor drives a copper-beryllium

\textsuperscript{4} TTF – TESLA Test Facility
alloy (CuBe) screw through an harmonic drive gear box what leads to final sensitivity below 1 Hz per step and to total static tuning range above 500 kHz (see Fig. 3.1 left).

![Fig. 3.1. TTF tuner block diagram (left) and its installation inside cryomodule (right) at FLASH facility. TTF tuner installation is located at the corresponding helium tank edge between the vessel and the cavity end dish, to allow the tuner for longitudinal tuning action. The stiffness of the whole assembly is close to 100 kN/mm.[10][12].](image)

The second solution, named as Blade tuner, is designed to be coaxial with the cavity and by means of elongation of the helium vessel, to deform the cavity geometry and consequently change the resonance frequency. The tuner assembly is mainly composed of two parts, the movement leverage and bending rings, as seen in Fig. 3.2.

![Fig. 3.2. The Blade tuner picture (left) and a schematic view of its assembly for TESLA cavity (right).[10][12].](image)

The leverage system amplifies the torque of the stepper motor, reducing dramatically the total movement and increasing the tuning sensitivity. A stepper motor unit is connected to the helium vessel tank and produces a rotation of the big arm in the tuner center. The movement of the arm induces the rotation of the bending rings equipped with thin titanium blades. The proper tuning provides compression or tension effect on the cavity structure.
The step motor tuners are commonly used for pre-detuning process what means initial tuning to cavity resonance frequency of order of 1.3 GHz. Since, the step motor based tuners are too slow to counteract the cavity deformation caused by 2 ms RF pulse, the fast frequency tuners based on piezo translators have been integrated into the both described slow tuning mechanisms. The piezoelectric actuators have been chosen in order to provide a nanometer resolution, high dynamic operation (several kHz), high forces (100 N) and high reliability [21], especially for operation in the radiation environment. The piezo integration of the TTF tuner has been obtained avoiding a complete redesign of the mechanical assembly. The mechanical part of TTF tuner, has been equipped with a compact titanium frame with 2 piezo parallel stacks – Saclay II tuner (see Fig. 3.3 left). The similar upgrade scheme has been performed for the Blade tuner design. The piezoelectric elements have been integrated by inserting two elements between one of end rings and the corresponding flange on the He vessel (see Fig. 3.3 right). This double stack configuration allows for keeping a spare actuator as redundant. If no replacement is needed, it is used as a sensor for mechanical vibrations, i.e. for microphonics noise identification.

![Fig. 3.3. The double stack piezos installed for TTF tuner design (left) – dark blue elements with grey end rods - and Blade tuner design (right) – dark grey elements with yellow end rods [10],[12].](image)

The main parameters of described frequency tuners are summarized in Tab. 3.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Saclay I</th>
<th>Saclay II</th>
<th>INFN Blade tuner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow tuning range [kHz]</td>
<td>440</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>Tuning resolution [Hz]</td>
<td>&gt;1</td>
<td>&gt;1</td>
<td>&gt;1</td>
</tr>
<tr>
<td>Fast actuator</td>
<td>piezo</td>
<td>piezo</td>
<td>piezo</td>
</tr>
<tr>
<td>No. of fast actuators/sensors</td>
<td>1-2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Fast tuning range [Hz]</td>
<td>&gt;500</td>
<td>1000</td>
<td>1200</td>
</tr>
</tbody>
</table>

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The TTF tuner design with piezo actuators was already developed and tested successfully for the Lorentz force detuning compensation [31][32][33][34] and therefore it was chosen for permanent installation of FLASH facility. Although, the first Blade tuner prototype design with piezo stacks was demonstrated successfully with its improved fast tuning range [35][36], it still needs a decision of on mass production for the RF linac technology. In spite of the fact, it is supposed to be a very attractive solution for the next generation experiments such as XFEL or even ILC\(^5\).

### 3.1.1. Piezoelectric Transducers

Piezoelectric transducers (PZT) have become increasingly popular in the vibration control applications. They are used as sensors and as actuators in the vibration control systems. They provide excellent actuation and sensing capabilities. The ability of piezoelectric materials to transform mechanical energy into electrical energy and vice versa was discovered over a century ago by Pierre and Jacque Curie. The French scientists discovered a class of materials that when pressured, generated electrical charge, and when placed inside an electric field, strained mechanically.

Piezoelectricity, which means “electricity generated from pressure” is found naturally in many monocristalline materials, such as quarts, tourmaline, topaz, and Rochelle salt. However, these materials are not generally suitable for actuators in the vibration control applications. Instead, man-made polycrystalline ceramic materials, such as lead zirconate titanate, can be processed to exhibit significant piezoelectric properties.

---

\(^5\) ILC – International Linear Collider [37]
Piezoelectric elements, most widely used as thin sheets, can be bounded to or embedded in composite structures. As actuators, they are mainly used for generating moment in the flexible structures, while as sensors, they are used for measuring strain. Piezoelectric actuators are also available as “stacks”, where many layers of materials and electrodes are assembled together, as seen in Fig. 3.4. The stacks generate large forces but small displacements in the direction normal to the top and bottom surfaces. Piezoelectric transducers are used in many applications such as structural vibration control, precision positioning, aerospace systems, and what is more, they have been critical to advancing research in nanotechnology [38][39]. The piezoelectric stacks are also the main part of the fast frequency tuners, where they are commonly used as actuators for the Lorentz force detuning active compensation.

### 3.1.2. Piezo Tuners at FLASH

The RF linac of FLASH accelerator is finished with 7 accelerating modules, each comprises of 8 superconducting cavities (after FLASH upgrade). The SC cavities have been divided into high (> 25 MV/m) and low gradients (< 25 MV/m). The high-gradient cavities have been installed inside ACC1, ACC6 and ACC7 accelerating modules and equipped with double stack piezo tuners from Physik Instrumente (PI) [40]. The low gradient cavities have been installed in ACC3 and ACC5 cryomodules and they are equipped with single piezo tuners. Half of them come from NOLIAC [41] and half from PI. The other cryomodules such as ACC2 or ACC4 are installed with step motor tuners only. The main parameters of FLASH piezo tuners are collected in Tab. 3.2.
As one can notice, the operation of PZT is limited by maximum tolerated voltage that can be applied to the element. It was experimentally proved that the operation above these conditions can lead to decrease in the lifetime of piezo elements or even break it when operated in such conditions for a long time [42]. In many cases, the piezo transducer should be monitored and protected by the control system. The piezo elements are high capacitive devices which is crucial from the driving circuit point of view. The typical capacitance of unloaded piezoelectric stack used for Saclay tuners, when measured at room temperature, is in the range of (6 ÷ 12) µF. The piezo capacitance is reduced approximately by factor of 3 for the cryogenic temperature operation at 2 K, as shown in Fig. 3.5. Carefully designed driving circuits should be used to meet such capacitive load. Most of all, the piezo driver should provide high-current, high-voltage output signal to allow piezo element to operate with enough stroke and actuating capabilities [43][44]. In most applications, the true bipolar, high power output signal is also recommended. The power consumption of the amplifier device should be also minimized. Special emphasis should be put on the power supply requirements, particularly the power supply has to be able to deliver very stable output voltage despite the pulse mode of the piezo driver operation.

---

6 The actuator capacitance are small signal values (measured at 1 V, 1000 Hz, 20 °C, unloaded)
The next section will summarize the development of high-voltage, high-current piezo drivers used for driving piezoelectric actuators. The special emphasis will be put on the piezo driver designed by DMCS\textsuperscript{7} group. The author of the thesis made his contribution to the first prototype laboratory tests as well as design and development of the 8-channel piezo driver for simultaneous compensation of the single cryomodule composed of 8 SC cavities.

\textsuperscript{7} DMCS – Dep. of Microelectronics and Computer Science
3.2. High Voltage, High Current Driving Circuits

Linear voltage power amplifiers are commonly used for driving the piezoelectric actuators. An extensive variety of commercial devices is available to suit most applications in the vibration control and positioning [39]. The major parameters to consider when selecting a voltage amplifier are:

1. Output current and voltage,
2. Maximum output power,
3. Bandwidth,
4. Slew rate.

The output voltage range is one of the crucial amplifier parameter. Although the amplifier should be capable of utilizing full rate voltage of the transducer, care should be taken to not over specify the amplifier. In the case of fault, or during periods of high disturbance, a voltage exceeding the maximum tolerated by the transducer will cause depolarization, that is, will begin the realign the piezoelectric dipoles within the material. An extended period of reverse over-voltage will depolarize the transducer completely. In some applications the transducers depolarize unavoidably when involved periodic high temperature that is greater than Curie temperature. In such cases, high voltage needs to be applied to the transducer after cooling and depolarizing it before the next usage. As the depolarization voltage is proportional to material thickness, thicker transducers will tolerate higher voltages.

The required output current can be approximated by modeling the transducer as a purely capacitive load, assuming conditions of maximum voltage and frequency, and it is specified by formula

\[ i_{\text{max}} = V_{\text{max}} \cdot 2 \cdot \pi \cdot C_p \cdot f_{\text{max}} \]  

(3.1)

where \( i_{\text{max}}, V_{\text{max}}, f_{\text{max}} \) and \( C_p \) mean the maximum output current, maximum voltage, maximum frequency of operation and piezo capacitance, respectively.

For the purely capacitive load driven by a sinusoidal excitation, the worst case power dissipation can be calculated from the following formula

\[ P = 4 \cdot V_s^2 \cdot C_p \cdot f_{\text{max}} \]  

(3.2)
where $\pm V_s$ is the supply voltage, $P$ is the worst case power dissipation in Watts, and $f_{\text{max}}$ is the maximum frequency of operation. Worst case dissipated power is of the most interest as it determines the internal heat generation. Sustained operation within the voltage, current and output power limits, while violating the maximum dissipated power, will overheat the amplifier and trigger a thermal shutdown.

Another important parameter, especially when enclosing the amplifier in a feedback loop, is the amplifier bandwidth of a dynamic transfer function. The majority of commercial amplifiers is voltage-feedback in construction. They are internally stabilized by dominant pole compensation, what results in second order transfer function

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{K \cdot \omega_{\text{amp}}^2}{s^2 + 2 \cdot \xi \cdot \omega_{\text{amp}} \cdot s + \omega_{\text{amp}}^2}$$

(3.3)

where $K$ is the DC gain, $\omega_{\text{amp}}$ is the corner frequency, and $\xi$ is the damping ratio.

The final parameter, slew-rate, is of little interest in the vibration control, but important to some positioning applications. In dynamic operation, the worst case slew-rate occurs at maximum voltage and frequency and as a result it limits the output voltage rate-of-change.

As it was already mentioned, the driving circuit for controlling the piezoelectric elements that are high capacitive load, needs to be carefully designed. As a proof of principle, the single channel prototype piezo driver device was simulated, designed and then tested in laboratory conditions [45].

The designed piezo driver unit is two-stage device. The first stage is based on pre-amplifier OP177 from Analog Devices and input circuit composed of overvoltage protection. The second stage is designed using power booster PB58 from Cirrus Logic (APEX). The PB58 is a high-voltage, high-current, general purpose amplifier, designed to provide voltage and current gain for a small signal. The main parameters of the device are collected in Tab. 3.3.

<table>
<thead>
<tr>
<th>Output current max. (A)</th>
<th>Supply voltage max. (V)</th>
<th>Slew rate typ. (V/µs)</th>
<th>Standby Current max. (mA)</th>
<th>Power dissipation max. (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>300</td>
<td>250</td>
<td>35</td>
<td>70</td>
</tr>
</tbody>
</table>

Including the power booster in the feedback loop of the driver pre-amplifier results in a composite amplifier with the extended output voltage range and current. The PB58 can be
also used without a driver in some applications, requiring only an external current limit resistor to function properly. The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by commonly used Bipolar Transistors. Internal feedback and gain set resistors are provided for a pin-strippable gain of 3. Additional gain can be achieved by a single external resistor. Compensation is not required for most driver gain configurations, but can be accomplished by a single external capacitor. The choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation provide enormous flexibility.

The global gain of the piezo driver unit for the design was set to 100 V/V, what makes it suitable for operation with low voltage input signals of order of ±1 V – the main requirement for LLRF digital control board of Simcon 3.1 or Simcon DSP [47]. The electrical scheme of designed piezo driver unit is shown in Fig. 3.6.

![Piezo driver circuit](image)

**Fig. 3.6.** Piezo driver circuit developed by DMCS group. The piezo driver consists of power amplifier PB58 from APEX in half bridge configuration (±150 V, 1.5 A).

The piezo driver circuit design was improved by the set of simulations using SPICE macro models of OP177 and PB58 devices. The sinusoidal excitation with frequency of 300 Hz
and amplitude of 1 V was chosen for the input signal $U_{in}$. The divider of the output voltage was applied for making it accessible to the typical ADC circuit. The output current was measured using $1 \Omega$ resistor. The example results of transient as well as the alternating current (AC) simulations are shown in Fig. 3.7 and Fig. 3.8.

![Figure 3.7](image)

**Fig. 3.7.** Transient simulation of DMCS piezo driver using SPICE models. The top waveform shows the input voltage amplitude, the middle top represents output voltage amplitude divided by factor of 100, the middle bottom shows output current amplitude ($I_{out} = V(R5:2)/1 \ [A=V/R]; 1 \Omega$ resistor is used as a current sensor). The bottom shows fast fourier transform of output voltage. The piezo driver was loaded with capacitance load of 2.5 $\mu$F and 4.5 $\mu$F. The vertical axis represents voltage, while the horizontal axis shows time in ms.
As one can realize, the piezo driver is suitable for driving the both piezo elements used for the fast frequency tuners. The output current amplitude is close to 1 A, what is reasonable according to capacitive load of 4.5 $\mu$F and can be compared to the analytical calculation using the equation (3.1). Since the piezo actuator driving signal frequency should not exceed 300 Hz (cavity half bandwidth, see section 2.3), the measured AC characteristic assures a stable operation of the piezo driver below the cut-off frequency, which is of order of 10 kHz.

The built prototype device was tested in the laboratory conditions in DESY research center. The main purpose of the tests was to check if the piezo driver unit will be able to work properly in conditions similar to accelerator environment. The power booster was equipped with dedicated external heat sink. The external heat sink was used according to the worst case power dissipation of order of 100 W, estimated using the equation (3.2). The first series of research were carried out to estimate the maximum operating ratings of the driver and were performed with amplifier without external case. The second series of research were performed after closing the amplifier with dedicated case and assembling it inside the industrial Eurocrate with a proper cooling system.
The measurements were performed using a dedicated control hardware platform as shown in Fig. 3.9. The control application running on SPARC CPU was used to setup the hardware platform of LLRF control board Simcon 3.1 using standard VME communication interface. The Simcon 3.1 LLRF control board was used to drive the piezo driver unit with low voltage driving signals of order of \( \pm 1 \) V. The piezo driver unit was loaded with capacitors of 2.47 \( \mu \)F, 3.3 \( \mu \)F and 5 \( \mu \)F, according to the piezo capacitance measurements presented in Fig. 3.5. The repetition rate of the driving signals was set to 10 Hz (nominal repetition rate of RF pulse for FLASH and XFEL). All research was carried out in room temperature of 25 °C.

During the experiment, the driving signal was set to different pulse width, starting from a half of sinusoidal exaction and finishing with several periods of full sine wave, as it is shown in Fig. 3.10. The piezo driver unit was operated within full range of output signal voltage amplitude without overcurrent conditions, see Fig. 3.11 right. The external cooling system was switched on to not exceed the maximum case temperature for PB58 power amplifier for the defined maximum operating ratings, (power supply \( V_s = \pm 130 \) V, up to four pulses of output signal voltage amplitude \( V_o = \pm 120 \) V, capacitance load \( C_p = 5 \) \( \mu \)F and 10 Hz repetition rate of the driving signal). The example results are shown in Fig. 3.11 left.
Fig. 3.10. The laboratory tests of single channel piezo driver circuit. The driving signal was generated using a single pulse excitation (A), and multi-pulse excitation with variable number of generated periods (B and C). C1 - output signal voltage amplitude of, C2 – input signal voltage amplitude of, C3 – output current amplitude [45].

Fig. 3.11. The results of piezo driver tests: a) temperature measurements with increased number of driving pulses, b) output signal amplitude and output current amplitude versus input signal amplitude [45].

It can be noted that, the designed power amplifier is capable of operating stably with full range of desired input signal range without gaining limitation. Moreover, the power tests carried out show that the system can operate stable without over-temperature conditions. The performed laboratory tests mainly proved that integration of 8 power amplifiers into the single Eurocard standard PCB board is possible. The next section will briefly describe the design of 8-channel piezo driver and its first tests after connecting to the fast frequency tuners for the Lorentz force detuning compensation at FLASH facility.
3.2.1. 8-channel Piezo Driver

The 8-channel piezo driver unit was developed for simultaneous tuning of 8 cavities equipped with the piezoelectric actuators. The piezo driver is based on PB51 power amplifiers having quite similar parameters as PB58, but more compact device package. It allows for integrating 8 power boosters on the single PCB board. Four external heat sinks were assembled to dissipate the output heat, each one was equipped with two amplifiers. The fact allows for finding some additional space for the integration of the output overvoltage protection circuits, the temperature monitoring sensors as well as the voltage suppressors for the power supply lines. The picture of designed PCB board and fully assembled piezo driver unit is shown in Fig. 3.12.

Fig. 3.12. The fully assembled 8-channel piezo driver is on the right side. The PCB board was assembled inside standard 6U box and ended with front panel. The high voltage output signals to piezo tuners are provided using TNC⁸ connectors located on the right side of the front panel. The three 8-channel D-SUB connectors on the left side of front panel are used to provide low voltage input signals as well as output voltage and output current monitoring signals [48][49].

⁸ TNC - connector is similar in size to a BNC except it features a threaded coupling nut and a typical operating frequency up to 11GHz. TNC connectors are widely used in telecommunications infrastructure applications.
The designed 8-channel piezo drivers have been laboratory tested with nominal and maximum operating conditions (long period power tests) at room temperature of 25 °C. The each output of the power amplifier has been loaded with 4 µF capacitors. The both operating conditions are listed below:

- **nominal operating conditions**: the power amplifiers gain $G_u = 100 \text{ V/V}$, the laboratory power supply - $V_{ss} = \pm 80 \text{ V}$, driving signal parameters: 4 periods of sinusoidal wave (amplitude $\pm 70 \text{ V}$, frequency 200 Hz, repetition rate of 10 Hz),

- **maximum operating conditions**: the power amplifiers gain $G_u = 100 \text{ V/V}$, the laboratory power supply $V_{ss} = \pm 130 \text{ V}$, driving signal parameters: 4 periods of sinusoidal wave (amplitude $\pm 120 \text{ V}$, frequency 200 Hz, repetition rate of 10 Hz).

During the nominal as well as maximum operating conditions the temperature of the power amplifiers case has been monitored. The temperature measured without external cooling system was close to 60 °C for the nominal operating conditions. When the external cooling system was turned on it was decreased to 45 °C. The temperature of the power amplifiers case was below 70 °C for the maximum operating conditions. For this conditions the external cooling system was permanently applied. During the tests, the main parameters of power supply unit have been defined and recalculated considering the usage of four 8-channels piezo drivers installed inside the single Eurocrate powered by external power supply (see Tab. 3.4).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>$\pm 100$</td>
</tr>
<tr>
<td>Output current</td>
<td>2</td>
</tr>
<tr>
<td>Output power</td>
<td>200</td>
</tr>
</tbody>
</table>

### 3.3. Lorentz Force Detuning Compensation with 8-channel Piezo Drivers

The LLRF control system was equipped with a digital piezo controller for controlling the piezos in FLASH facility. It operates closely with an RF controller and computes detuning according to the RF signals [50][51]. It is assumed that detuning (that is due to Lorentz force) is repeatable in successive pulses. The compensation pulse is a single period of sinusoidal waveform with modulated amplitude and time. The compensation pulse occurs before the RF pulse. It is important to note, that other shapes of pulse can be also applied. The pulse frequency is fitted to the mechanical resonance of the cavity (for
TESLA cavities, it is about 300 Hz). Based on the estimated detuning, the parameters of compensating pulse are calculated for the next RF pulse. The Simcon DSP board was used for signal processing and generation. It is equipped with FPGA circuit and analog inputs and outputs (14 bit ADCs and DACs). The compensating pulses are generated in a multichannel programmable generator and amplified by a piezo driver unit (see Fig. 3.12).

The developed piezo control system was evaluated in the FLASH accelerator during the study period (August 2007). The piezos were installed in three of six accelerating modules ACC3, ACC5 and ACC6. The piezo control system was installed and connected to the piezos, as seen in Fig. 3.13.

![Fig. 3.13. The piezo control system installation at FLASH (left). The block diagram of the control system connected to piezo tuners (right).](image)

Before the measurements, the capacitance of all piezos was measured and verified (see Fig. 3.5). The detuning was measured in all cavities operating without any compensation. The accelerator was operated with a high gradient. During the RF pulse, the detuning was of order of 300 Hz (depending on the cavity). After measurements without piezo compensation, the piezo control system was turned on. Both types of piezos were driven successfully by the control system equipped with the designed driving circuits. After tuning manually the parameters of the compensating pulse, the detuning during the RF pulses was reduced significantly (below 10 Hz – see Fig. 3.14). The parameters of the
compensating pulses varied slightly depending on the cavity (the pulse amplitude was about 50 V, the pulse given to the piezo was about 2 ms in advance of RF pulse).

After the Lorentz force detuning compensation for ACC 6 module was performed successfully, the piezo control system was reconfigured to compensate simultaneously 16 cavities. Since, the LLRF driving board was equipped with only 8 DACs output, the compensation pulse parameters were set experimentally to tune each of 2 cavities to the same parameters. The example histograms of the Lorentz force detuning compensation are shown in Fig. 3.15.

Fig. 3.14. The detuning in ACC 6 without compensation (red) and with compensation (green). Gradient SP = 15 MV/m, Pfor = 220 kW, rep = 5 Hz. Cavity 5 is not compensated due to known problem with mechanical fixing [48][49].

Fig. 3.15. The Lorentz force detuning histograms for ACC3 and ACC5 accelerating modules operating with high accelerating field gradients [49].
To conclude, the main operation parameters of the designed driving circuit – 8-channel piezo driver can be summarized as:

- suitably operating with both types of installed piezo tuners from NOLIAC and PI,
- having a power stage gain of $G_u = 100 \, \text{V/V}$, what makes the unit operable with small input signals of $\pm 1 \, \text{V}$ provided by LLRF control boards,
- having a power amplifier bandwidth of 10 kHz, which is enough for generating the compensation signal of frequency similar to the half bandwidth of the cavity,
- having a possible output voltage level of $\pm 100 \, \text{V}$, which allows the Lorentz force detuning compensation for high accelerating field gradients above 25 MV/m,
- having 8 independent channels integrated into a single PCB board – the possibility of integration was mainly proved by the carried thermal tests,
- having crosstalk between driving circuit outputs above 60 dB, what is more than the measured crosstalk along the accelerating module – (see Appendix C:).

In addition, the tests that were carried out proved that **it is possible to perform the simultaneous Lorentz force detuning compensation for each superconducting resonant (SCRS) cavity over a single accelerating module using a carefully-designed driving circuit of fast frequency tuners based on the piezoelectric elements.** This is the proof of the first thesis of this dissertation.
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4. DIGITAL CONTROLLER DEVELOPMENT

Currently, most of the modern control systems are based on digital processing unit equipped with fast ADC and DAC [52][53][54]. The ADC circuits are used to measure the plant\(^9\) response, while the DAC circuits are used for driving the plant with desired correction signal. First of all, when developing such systems, the main requirements for the control system should be defined. What is more, the driving signal as well as controller transfer function should be investigated and validated with the open loop, then closed loop operation of the controller. To realize the cavity tuning to resonance of 1.3 GHz and keep it as long as possible at a level lower than 10 Hz, the multi-channel analog driving circuit should be equipped with a digital controller. This paragraph introduces the development stages of the fast frequency controller. Since, the cavity detuning measurement is the most critical input to the controller (cavity response), its main measurement techniques are described briefly. The special emphasis is put on the hardware implementation using modern FPGA devices, which are the main part of LLRF control systems [55][56]. Moreover, the novel approach to the automatic control of frequency tuners with the use of DC characteristics of piezo element is discussed and the first results of carried out tests are presented.

4.1. Piezo Control Requirements

The control system for the fast frequency tuners should be designed according to the general requirements, which are strongly recommended for FEL operation of FLASH as well as XFEL. Most requirements were clarified during study weeks dedicated mainly to research and development of LLRF control subsystem. All the research was carried out with contribution of the author of the thesis and can be easily restored using history of FLASH logbook [57]. The most important requirements are listed below.

1. *Compensate of dynamic Lorentz force detuning* (\textbf{LFD}) over the flat top of RF pulse in range below 10 Hz for high accelerating field gradients up to above 30 MV/m [58][59] (*the dynamic detuning is measured using the difference value between*

\(^9\) Plant – set of actuator, process and sensor
start and end of the flat top duration, see Fig. 2.8 top left)—according to the Lorentz force detuning coefficient of 0.414 Hz/(MV/m)^2 (see Fig. 2.8 top right), it gives around 400 Hz of cavity resonance frequency shift that needs to be corrected for gradients of 35 MV/m (the compensation signal should be investigated and its optimized parameters should be automatically applied by digital controller).

2. Allow suitable operation for maximum repetition rate of RF pulse of 10 Hz – the digital controller should be able to update the compensation pulse parameters between successive RF pulses with frequency below the maximum RF pulse repetition rate.

3. Allow for cavity tuning and by-passing in limited range of ±1 kHz instead of using step motors – it can extend significantly the lifetime of slow frequency tuners based on the step motors.

4. Minimize the RF control efforts – it was experimentally proved that klystron power for a single cavity can be increased up to 25% when cavity detuning is of order of 200 Hz (see Fig. 2.8 bottom), it may play a crucial role when operated close to klystron saturation and therefore it should be taken into consideration by the tuning system.

5. Assure piezo lifetime for at least 20 years of operation (piezo must be protected and monitored) [42] – the overvoltage and over-current protection should be generally provided by the driving circuit, for the monitoring purpose the second piezo operating as a sensor can be efficiently used (see Appendix B:).

6. Compensate the additional mechanical vibrations caused by the piezo compensation pulse – at higher repetition rates of RF field pulse (up to 10 Hz) the residual vibrations from the previous RF pulses can be substantial, what may result in unexpected accelerating field errors, for that purpose, the piezo elements operating as piezo sensors should be applied (piezo feedback) (see Appendix B:).

4.2. Typical Control Scheme

The design of the fast frequency tuners control system should start with a proper definition of the compensation pulse. The chosen strategy is to duplicate the kind of excitation induced by the RF field pulse itself (see Fig. 2.6). As a proof of principle, the shape of sinusoidal wave has been used. The half and full periods of sine wave were tested. Most of all, the main parameters of the chosen compensation pulse have been investigated.
As it is shown schematically in Fig. 4.1, the cavity detuning is decoupled into two main parameters of the driving signal [10][12]. The time position of the compensation signal at the start of the RF field pulse plays a crucial role as it is capable of compensating a static detuning (the static detuning is measured using mean value of flat top duration of detuning curve, see Fig. 2.8 top left). Its value is variable from cavity to cavity and greatly depends on the time delay of mechanical wave propagation along the cavity structure. For most cavities, the 2 ms time advance to the RF pulse is suitable and therefore it may be treated by controller as a constant with some fine tuning range of hundreds of $\mu$s for particular cavities. The most important parameter of the driving signal is its amplitude. The amplitude has strong impact on the dynamic detuning and its value, as it was already experimentally proved [10], mainly depends on the accelerating field gradient. The last parameter, the compensation pulse width, was fixed to 4 ms and it corresponds to the cavity mechanical resonance frequency of order of 250 Hz.

The first tests of the driving signal have been performed using a half period of sinusoidal wave (1st compensation scheme). The tests have been carried out on the accelerating module ACC6 when it was installed in MTS. The MTS facility was built to supports tests of the new fabricated cryomodules. The MTS allows for testing cavities independently with high accelerating field gradients operation even if low gradient cavities along the accelerating module were switched off to avoid quench conditions. The corresponding cavities were operated with different accelerating field gradients ranging from 20 MV/m to

\[ \text{quench} \] – the cavity state when it is operated above the accelerating field gradient limit

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33 MV/m. The Lorentz force detuning was compensated for less than 10 Hz using a proper amplitude and fixed value of 2 ms of time advance to the RF pulse for each cavity. The example results for high gradient cavities of ACC6 are shown in Fig. 4.2 top.

Fig. 4.2. The dependence of piezo compensation pulse amplitude, applied for Lorentz force detuning compensation, versus accelerating field gradient using a half of sine drive (top) and full period of sine drive (bottom). The vertical axis has been rescaled for visualization purpose.
High gradient measurements were repeated with full period of sinusoidal excitation (2\textsuperscript{nd} compensation scheme) when accelerating module ACC6 was installed permanently inside the FLASH facility. The cavities were operated with average accelerating field gradients of 25 MV/m. The individual setup of high gradients cavities was not possible due to the fact that the single cavity quench state switched off the RF field inside all cavities along the module. The example results are shown in Fig. 4.2 bottom. It can be observed that applying a full sine wave shape as a compensation pulse reduced the demand amplitude by factor of two. Since the piezo elements are very susceptible to overvoltage conditions, all the next experiments with controller development were carried out using 2\textsuperscript{nd} compensation scheme.

### 4.3. Lorentz Force Detuning Computation

Measuring the Lorentz force detuning is the most important part for the fast frequency tuners controller as it is used for estimating the cavity response to the applied compensation signal. The SC cavity detuning can be measured by various methods [60][61]. The most popular analog method is based on the phase detector circuit. A phase detector device compares the phase of cavity output signal (electrical field induced inside the cavity and measured by the RF pickup probe) with the phase of cavity input signal (power transmitted to the cavity from klystron). Phase detection is performed using dedicated RF mixer followed by the low-pass filter. The low-pass filter is used to cut-off the intermediate products from the mixer output signal. The mixer output signal is directly related to the phase difference $\Delta \varphi$ which is proportional to the shift of cavity resonance frequency also called cavity detuning. The block diagram of the measurement circuit is shown in Fig. 4.3.
Since the modern control systems are generally based on DSP or FPGA devices, the digital computation of cavity detuning is strongly recommended. The principle of digital detuning computation is to measure the cavity input and output RF signals. First of all, the RF signals are down-converted from 1.3 GHz frequency to intermediate frequency of 250 kHz by dedicated RF mixers, see Fig. 4.4 right. The RF mixer output signal is sampled by ADC converter 4 times faster than intermediate frequency and as a result the four corresponding samples: I, Q, negative I and negative Q are collected, then demodulated to complex signal envelope (I and Q means In-phase and Quadrature), see Fig. 4.4 left. The complex field vectors can be used to model the cavity behavior and during further processing they can be used to compute the demand cavity parameter.
4.3.1. Cavity Baseband Equation

The typical RF system is composed of superconducting cavity driven by RF klystron and fed with electron beam using RF gun. The RF power is transmitted to the cavity via transmission line (typically waveguide or coaxial cable) and a directional coupler. The simple RF system composed of single cavity can be described by equivalent circuit model, as seen in Fig. 4.5.

The model assumes that the excitation of the cavity by the generator and by the beam is described by constant current sources $I_g$ and $I_b$. A circulator is inserted into the transmission line which directs the RF wave from the generator to the cavity and deviates any waves reflected at the cavity to a matched load with impedance $Z_0$. This is necessary since the klystron may be destroyed by reflected waves. The superconducting cavity is modeled using LCR circuit. The input coupler is used for feeding a cavity with RF power. The coupling from the klystron output of the transmission line and from the transmission line to the cavity side is represented by the lossless transformer. The input coupler of the...
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cavity has a transformation ratio of 1:n. The study of cavity behavior is possible when the circuit model is transferred to the cavity side of the directional coupler, see Fig. 4.6. The voltages, currents and impedances can be transferred to the secondary side of the ideal transformer using well known transformation equations

\[
\begin{align*}
V_2 &= n \cdot V_1 \\
I_2 &= \frac{1}{n} \cdot I_1 \\
Z_2 &= n^2 \cdot Z_1
\end{align*}
\]  

(4.1)

where \(V_1, I_1, Z_1\) represent voltages, currents and impedances on the primary side of the transformer.

![Fig. 4.6. The circuit model of the RF system converted to the cavity side using the ideal transformer equations.](image)

Using the circuit topology shown in Fig. 4.6, the following differential equation can be derived

\[
\frac{d^2 V_c}{dt^2} + \frac{1}{R_L C} \cdot \frac{dV_c}{dt} + \frac{1}{LC} \cdot V_c = \frac{1}{C} \frac{dl_c}{dt}
\]  

(4.2)

where \(R_L, Z_{ext}, V_c\) and \(I_c\) mean loaded shunt impedance, external load impedance, cavity voltage and cavity current, respectively. The cavity voltage and current are considered as sine signals with phase and amplitude modulation. The loaded shunt impedance is a result of parallel connection of cavity parameter \(R\) and loaded external impedance and it is equal to
The cavity current may be derived using Kirchhoff rule applied for the cavity node and it is equal to

\[ I_c = I_g' - I_b \]  \hspace{1cm} (4.4)

where \( I_g' \) means the generator current transformed to the cavity side.

Since the equation (4.2) can be expressed by typical cavity characteristics, the short description of used parameters and their typical values for TESLA cavity are shown in Tab. 4.1. The differential equation (4.2) can be rewritten using half bandwidth (\( \omega_{1/2} \)) of the cavity

\[ \frac{d^2V_c}{dt^2} + 2\omega_{1/2} \frac{dV_c}{dt} + \omega_0^2 V_c = 2\omega_{1/2} R_L \frac{dl_c}{dt} \]  \hspace{1cm} (4.5)

where

\[ \omega_{1/2} = \frac{\omega_0}{2Q_L} \]  \hspace{1cm} (4.6)

When studying the cavity behavior with klystron power and beam current, small terms in second order derivatives as well as carrier frequency term may be neglected according to

\[ \begin{cases} \frac{d^2V_c}{dt^2} \ll \omega_0^2 V_c \\ \frac{dV_c}{dt} \ll \omega_0^2 V_c \\ \int_{t_2}^{t_1} \frac{dl_c}{dt} dt \ll \int_{t_2}^{t_1} \omega_0 l_c dt \end{cases} \]  \hspace{1cm} (4.7)

and the cavity baseband equation can be expressed as
\[ \frac{dV_c}{dt} + (\omega_{1/2} - j\Delta\omega)V_c = 2\omega_{1/2}R_LI_c \] (4.8)

where
\[ \Delta\omega = \omega_0 - \omega \] (4.9)

Since the RF signals are measured as voltage, the cavity equation can be forwarded to voltage driven representation
\[ \frac{dV_c}{dt} + (\omega_{1/2} - j\Delta\omega)V_c = 2\omega_{1/2} \frac{\beta}{\beta + 1} V_{\text{for}} \] (4.10)

which is valid for both normal-conducting and superconducting cavities.

Tab. 4.1. The main cavity characteristics for TESLA technology.

<table>
<thead>
<tr>
<th>Resonance frequency ( f_0 )</th>
<th>( \omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}} )</th>
<th>( f_0 = 1.3 \text{ GHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quality factor and input coupling factor</td>
<td>( Q_0 = \frac{\omega_0 W}{P_{\text{diss,cav}}} = \omega_0 RC = \frac{R}{L\omega_0} )</td>
<td>( Q_0 \sim 1\text{e10} ) (unloaded quality factor)</td>
</tr>
<tr>
<td></td>
<td>( Q_{\text{ext}} = \frac{\omega_0 W}{P_{\text{diss,cav}}} = \omega_0 n^2 Z_0 C )</td>
<td>external load quality factor</td>
</tr>
<tr>
<td></td>
<td>( \beta = \frac{P_{\text{diss,ext}}}{P_{\text{diss,cav}}} = \frac{Q_0}{Q_{\text{ext}}} = \frac{R}{n^2 Z_0} )</td>
<td>( \beta &gt; 3000 ) (input coupling factor)</td>
</tr>
<tr>
<td></td>
<td>( Q_L = \frac{Q_0}{1 + \beta} )</td>
<td>( Q_L \sim 3\text{e6} ) (loaded quality factor)</td>
</tr>
</tbody>
</table>

Shunt impedance \( r \) and normalized shunt impedance \( (r/Q) \)

\[ R = \frac{1}{2} r = \frac{1}{2} \frac{r}{Q} Q_0 \] cavity parameter

\[ n = \frac{R}{\beta Z_0} \] ideal transformer ratio

\[ R_L = R || n^2 Z_0 = \frac{R}{1 + \beta} = \frac{1}{2} \frac{r}{Q} Q_L \] \( R_L \sim 1554 \text{ M}\Omega \) (loaded shunt impedance)

When considering the superconducting cavity with the large coupling factor as for TESLA technology
\[ \beta \gg 1 \] (4.11)

the cavity equation can be simplified to
The cavity detuning can be derived using I and Q representation of complex vector fields (Cartesian coordinates) or using amplitude (A) and phase (P) representation (Polar coordinates). The next section will introduce briefly the both methods of detuning computation with special emphasis on the hardware implementation purpose.

### 4.3.2. Cartesian and Polar Coordinates Conversion

The cavity equation (4.12), which is represented in Cartesian coordinates, can be simplified to

\[
\frac{dV_c}{dt} + j\Delta\omega V_c = 2\omega_1/2V_{for} \tag{4.13}
\]

assuming that the cavity voltage signal at the beginning of the RF pulse is very small. The real and imaginary parts of the complex field vectors \( V_c \) and \( V_{for} \) can be replaced by I and Q components, since they are always sine signals with phase and amplitude modulation.

As a result, the cavity detuning can be calculated using formula [61]

\[
\Delta\omega = \left( \frac{\frac{dI_c}{dt} - coeff \cdot I_{for}}{I_c^2 + Q_c^2} \right) \cdot Q_c + \left( \frac{\frac{dQ_c}{dt} - coeff \cdot Q_{for}}{I_c^2 + Q_c^2} \right) \cdot I_c \tag{4.14}
\]

where cavity voltage \( V_c \) and generator voltage \( V_{for} \) are as follows

\[
\begin{cases}
V_c = I_c + jQ_c \\
V_{for} = I_{for} + jQ_{for}
\end{cases} \tag{4.15}
\]

The parameter \( coeff \) can be treated as a constant value and it is defined as

\[
coeff = 2\omega_1/2 \tag{4.16}
\]

The cavity baseband equation (4.12) can be converted to Polar coordinates and it is expressed by the following formula [61]

\[
(|V_c|e^{j\varphi_c} + je^{j\varphi_c}\phi_c|V_c|) + (\omega_1/2 - j\Delta\omega)(|V_c|e^{j\varphi_c}) = 2\omega_1/2(|V_{for}|e^{j\varphi_{for}}) \tag{4.17}
\]
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where

\[
\begin{align*}
V_c &= |V_c|e^{j\varphi_c} \\
V_{for} &= |V_{for}|e^{j\varphi_{for}}
\end{align*}
\]  

(4.18)

The equation (4.17) can be separated to

real

\[|\dot{V}_c| + \omega_{1/2}|V_c| = 2\omega_{1/2}V_{for}\cos(\varphi_{for} - \varphi_c)\]  

(4.19)

and imaginary parts

\[|\dot{V}_c|\varphi_c - \Delta\omega|V_c| = 2\omega_{1/2}V_{for}\sin(\varphi_{for} - \varphi_c)\]  

(4.20)

and since the only imaginary part has a detuning term, the real part may be neglected.

Finally, the cavity detuning may be calculated using formula [61]

\[
\Delta\omega = \varphi_c - \text{coeff} \frac{|V_{for}|}{|V_c|} \sin(\varphi_{for} - \varphi_c).
\]  

(4.21)

where \(\varphi_c, \varphi_{for}\) mean the phase of cavity voltage and generator voltage.

Both detuning computation methods have been tested using Matlab engineering software. The example computation results are shown in Fig. 4.7.

Fig. 4.7. Detuning computation methods using different variations of cavity baseband equation.

As one can realize, the computation differences between both methods are very small and they may be neglected for the flattop region. Both methods have been carefully analyzed.
and finally the Polar coordinate conversion has been chosen for the hardware implementation. The method was chosen for optimized number of hardware resources usage needed for final detuning computation, see Tab. 4.2.

Tab. 4.2. The preliminary estimation of hardware resources for implementation of both detuning computation methods.

<table>
<thead>
<tr>
<th>Hardware resources</th>
<th>Cartesian coordinates</th>
<th>Polar coordinates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplier</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Divider</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Adders/subs</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>Differentiator</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

4.3.3. Coupler Directivity Calibration

The calibration of input coupler directivity is very important when considering the measurements of the cavity detuning parameter. Since the forward (power transmitted to the cavity) $V_{\text{for}_m}'$ and reflected (power reflected from the cavity) $V_{\text{ref}_m}'$ signals to a single cavity are measured from the directional couplers side (not cavity side), one should assume that the both signals include the crosstalk caused mainly by the none ideal directional couplers [61]. If $V_{\text{for}}'$, $V_{\text{ref}}'$ and $V_c'$ are the forward, reflected and cavity voltage signals respectively, they meet the following equations

$$
\begin{align*}
V_c' &= V_{\text{for}}' + V_{\text{ref}}' \\
V_{\text{for}}' &= aV_{\text{for}_m}' + bV_{\text{ref}_m}' \\
V_{\text{ref}}' &= cV_{\text{for}_m}' + dV_{\text{ref}_m}'
\end{align*}
$$

(4.22)

where $a$, $b$, $c$ and $d$ are the calibration coefficients to be decided. Since the $V_c'$, $V_{\text{for}_m}'$ and $V_{\text{ref}_m}'$ are directly measured by the ADCs, $M$ and $N$ may be calculated by linear fitting using the following equations

$$
V_c' = M \cdot V_{\text{for}_m}' + N \cdot V_{\text{ref}_m}'
$$

(4.23)

where

$$
\begin{align*}
M &= a + c \\
N &= b + d
\end{align*}
$$

(4.24)

When the RF power is switched off, $V_{\text{for}}'$ will be zero. In this case once can calculate
When considering that $V_{\text{for}}'$ is similar to a step function and the cavity voltage is very small but the derivative is very large at the time when the RF pulse start ($t->0$), the cavity baseband equation (4.12) may be approximated as

$$aV'_{\text{form}} + bV'_{\text{ref}} = 0 \rightarrow b = -\frac{aV'_{\text{form}}}{V'_{\text{ref}}} \quad (4.25)$$

From the equations above, the calibration coefficients $a, b, c$ and $d$ may be calculated. The example computation results are shown in Fig. 4.8.
Fig. 4.8. Measured RF signals with (top) and without calibration (middle). The cavity detuning computed with and without calibration (bottom).
It can be point out that, the computation error caused by none ideal input couplers may be sufficient and result in detuning error of about 150 Hz. Since such computation error cannot be accepted by the controller, the calibration procedure is essential.

### 4.3.4. Hardware Implementation

The hardware implementation of detuning computation has been realized using LLRF control board of Simcon DSP, see Fig. 4.9. The board is equipped with high performance FPGA device Virtex II Pro from Xilinx, DSP Tiger Shark processor from Analog Devices and fast ADCs and DACs converters. Moreover, the other peripherals such as: external SRAM memory, digital input/output circuits, fast Ethernet interface or even optical modules have been added to flexible board extensions as well as fast data preprocessing and synchronization. The Simcon DSP board is designed in VME\(^{11}\) standard that means the main communication is based on VME bus interface through dedicated bus controllers and arbiters.

![Fig. 4.9. The LLRF control board of Simcon DSP. The board is equipped with 10 ADCs and 8 DACs converters for sensing and driving purposes. The FPGA and DSP devices support fast data preprocessing as well as various algorithms computation using system clocks up to 100 MHz.](image)

To verify and debug the most crucial detuning computation blocks, the simple hardware simulator has been designed, as seen in Fig. 4.10. It is composed of DOOCS server, Matlab

\(^{11}\) VME – Versa Module Eurocard
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software, Integral Interface communication module, Input and Output Memory Blocks, detuning Algorithm Computation block and Trigger and Strobe generators. The DOOCS server is used to provide raw data from monitoring ADCs of LLRF control system. The raw data is measured from RF probes after down-conversion to IF frequency. The Matlab software is used for communicating with DOOCS servers and hardware simulator. Moreover, it is used for data pre-processing and analyzing. The Mexsol based library for communicating with DOOCS server as well as hardware platform. The Integral Interface module is implemented inside FPGA device to make accessible user defined memory locations as well as registers using VME bus interface [62]. The Input and Output Memory Blocks are used to store the simulator input data and the algorithm computation output data. The trigger and strobe generators are added to simulate the timing signals distributed for the real LLRF control system. The trigger signal starts the new RF field pulse. The strobe signal is used for sampling the raw data from ADCs. For the simulation purpose, ADCs are replaced with Input Memory Blocks.

Fig. 4.10. The block diagram of hardware simulator used for detuning computation validation and debugging.

Since the Simcon DSP board is dedicated for multi-cavity configuration (10 ADCs, 8 DACs), the multichannel detuning computation has been implemented. The idea of the parallel computation blocks that could be used independently for each cavity was neglected, since it consumes the hardware resources multiplied by the number of cavities. To minimize the hardware resources, the serial solution was decided. Its main structure is shown in Fig. 4.11. When the samples from each cavity are ready for the input mux block, the valid signal is generated and the corresponding sample from each cavity is shifted into the computation pipeline word by word with single clock latency. The pipeline depth is equal to the number of cavities used for the computation. The valid signal is provided to inform the pipeline blocks that a new sample from each cavity is ready. Moreover, it is used to activate the output demux block to start conversion of serial data to parallel data.
The chosen computation stage of detuning algorithm may be debugged using multiplexer circuit inserted between each computation block and output demux block.

For the computation purpose, the following variation of equation (4.12) has been used

\[
\Delta \omega = \left( \phi_c - \text{coeff} \frac{|V_{\text{for}}|}{|V_c|} \sin(\phi_{\text{for}} - \phi_c) \right) \cdot \frac{1}{2\pi}
\]  

(4.27)

where \( \Delta \omega \) in this case, means the normalized detuning. The detuning computation block has been coded in VHDL description language and its main structure is shown in Fig. 4.12.

All the computations are done using 18-bit numbers in 2’complement representation using universal mathematical library for high energy physics experiments mainly developed in [63]. The IQ demodulators of probe (cavity voltage), forward and reflected signals are used to get I and Q components of raw data from ADCs. The Forward/Reflected Calibration block is used to attenuate the crosstalk between the forward and reflected waves measured on the directional coupler side (see section 4.3.3). The Probe/Forward Coordinate Conversion block is used to translate the I and Q components into amplitude and phase representation. Finally, the partially computed detuning (detn1 and detn2) is calibrated and used for further data analyzes.

Fig. 4.11. The pipeline solution for multi-channel configuration of detuning computation.
The key components of cavity detuning computation are briefly described and summarized in the following subsections.

### 4.3.4.1. IQ Demodulation

The IQ demodulator block takes data from ADCs. The data read from ADCs is modulated using In-phase and Quadrature modulation scheme which assumes that the four corresponding samples are grouped as follows: I, Q, negative I, negative Q. The I and negative I as well as Q and negative Q samples should have the same absolute values [64]. Since the RF signals are down-converted by none linear down-converters and sampled using ADC converters, the offset error is always presented between the positive and negative components [65][66]. The offset calibration is realized by average value between the current and previous samples of each component. When the positive component is sampled, the offset is subtracted from the current sample. When the negative component is expected, the current sample is subtracted from the offset value. The I and Q components are calculated using the following formulas

\[
\begin{align*}
I(n) &= P\_I\_DATA(n) - offset(n) \\
Q(n) &= P\_I\_DATA(n) - offset(n)
\end{align*}
\]

(4.28)

\[
\begin{align*}
I(n) &= offset(n) - P\_I\_DATA(n) \\
Q(n) &= offset(n) - P\_I\_DATA(n)
\end{align*}
\]

(4.29)

where offset is defined as
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\[
\text{offset}(n) = \frac{P\_I\_DATA(n) + P\_I\_DATA(n - 2)}{2}
\]  

(4.30)

and \(n, \ldots, n-2\) means current and delayed samples of discrete time domain data. The example hardware computation results of I and Q components of cavity voltage signal are shown in Fig. 4.13.

Fig. 4.13. The cavity voltage signal taken from monitoring ADCs (raw data) (top) and its demodulation to I and Q components complex field vector (bottom). The floating point data has been converted to 18 bits 2’complement data for hardware computations purpose.

4.3.4.2. Forward/Reflected Calibration

The hardware implementation of forward and reflected signals calibration procedure has been reduced to the multiplication of complex field vectors. The calibration coefficients are first calculated using Matlab software engineering, then they are sent to the...
hardware simulator using complex number representation. The calibration procedure is realized using formula

\[ V_{for} = (I_{for} + jQ_{for}) \cdot (a_{for} + jb_{for}) + (I_{refl} + jQ_{refl}) \cdot (c_{refl} + jd_{refl}) \]  \hspace{1cm} (4.31)

where \(a_{for}, b_{for}, c_{refl}, d_{refl}\) mean the calibration coefficients of forward and reflected power and \(I_{for}, Q_{for}, I_{refl}, Q_{refl}\) mean the In-phase and Quadrature components of forward and reflected power.

The block diagram of hardware implementation of calibration procedure is shown in Fig. 4.14.

![Block diagram of calibration procedure](image)

**Fig. 4.14.** The calibration procedure implemented in FPGA. The first stage is multiplication by calibration coefficients. The second stage is adding the real and subtracting the imaginary parts of complex vectors. The third stage is adding real and imaginary parts of complex vectors.

### 4.3.4.3. **Probe/Forward Coordinate Conversion**

The most popular method of converting rectangular to Polar and back Polar to rectangular coordinates conversion is based on COordinate Rotation DIgital Computer (CORDIC) algorithm. The COORDIC algorithm provides an iterative method of performing vector rotations by arbitrary angles using only shifts and adds [67][68][69][70]. It may be operated in one of two modes. The first mode rotates the input vector with specified angle (given as an argument). The second mode rotates the input vector to the x axis while recording the angle required to make that rotation. The result of the vectoring operation is a rotation angle (\(z\) component) and the scaled magnitude of the original vector (the \(x\) component of the result). In vectoring mode, the CORDIC equations are
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\[
\begin{align*}
\begin{cases}
x(n + 1) &= x(n) - y(n)d(n)2^{-n} \\
y(n + 1) &= y(n) + x(n)d(n)2^{-n} \\
z(n + 1) &= z(n) - d(n)\tan^{-1}(2^{-n})
\end{cases}
\end{align*}
\]

where

\[
\begin{align*}
\begin{cases}
d(n) &= 1 \quad \text{when } y(n) < 0 \\
d(n) &= -1 \quad \text{when } y(n) > 0
\end{cases}
\end{align*}
\]

and \(x(n), z(n)\) mean magnitude and phase of complex field vector, respectively.

The CORDIC computer has been decided to be accomplished with 12 iterations in order to minimize the computation error for amplitude and phase. The latency of implemented block may be easily reduced by factor of two using shift registers (rotators) operating on the both edges of the system clock. Since the typical CORDIC base angle range is of order of \(\pm\pi/2\), its range has been extended to \(\pm\pi\) range. The CORDIC base angle extension was decided to avoid sine value saturation which is needed for the final detuning computation. The base angle values are calculated in Matlab software engineering, then converted to fixed point representation and finally stored in lookup table of FPGA device. The example hardware computation results for the cavity voltage amplitude are shown in Fig. 4.15.
4.3.4.4. Derivative

The derivative computation may be realized by simple numerical method. The main idea of the method is to subtract the current and previous samples and divide the result by sampling period of time. Since, the I and Q components may be noisy, mainly due to analog to digital conversion effect, the classic method of derivative computation of its product (phase) cannot be applied directly. To improve the derivative computation and minimize the input signal noise effect, the averaging Finite Impulse Response (FIR) filter has been introduced [61]. For the derivative computation, the filter coefficients are set to [-1,1]. To minimize the input signal noise, the 32 taps of the FIR filter have been used. The structure has been optimized for hardware implementation, replacing the multiplications by positive and negative coefficients with the simple buffers and inverters. Moreover, the filter structure has been rebuilt to meet the pipeline computation with additional shift registers and serdes (serializer deserializer) components, as shown in Fig. 4.16. Finally, the derivative FIR filter depth has been reduced to 3 by single tap Infinite Impulse Response.
(IIR) low pass filters applied for the input signals. The latency of 8-taps derivative filter is equal to 6 system clocks.

![Diagram of multichannel, pipelined derivative filter](image)

**Fig. 4.16. The block diagram of multichannel, pipelined derivative filter.**

### 4.3.4.5. Division

The numerical methods for division computation are commonly based on slow (restoring, non-performing restoring, non-restoring and SRT (Sweeney, Robertson, Tocher) and fast division algorithms (Newton-Raphson or Goldschmidt) [68]. Slow division algorithms produce one digit of the final quotient per iteration. Fast division methods start with a close approximation of the final quotient and produce twice as many digits of the final quotient in each iteration. All mentioned methods are based on the form

\[ Q = \frac{N}{D} \quad (4.34) \]

where Q means quotient, N numerator (dividend) and D denominator (divisor). Since, the described methods are all iterative and for 18-bit numbers division need at least a latency of more than 10 system clocks, the division algorithm has been implemented by simple linear interpolator of 1/x function multiplied by dividend component, see Fig. 4.17. The latency for single cavity computation of used solution was reduced to 4 system clocks.
4.3.4.6. Sine Approximation

The proposed solution is based on the simple interpolator composed of a lookup table with pre-calculated sine values. The address of lookup table memory is calculated using phase subtraction of forward and probe signals, according to detuning algorithm. The lookup table depth has been reduced to 4 k words, since the first 6 bits of the subtraction result have been investigated to be less significant. The block diagram of sinus approximation is shown in Fig. 4.18. The latency of proposed solution is equal to 3 system clocks.

4.3.4.7. Final Detuning Computation

The final detuning computation is accomplished with single subtraction of detn1 and detn2 components [71][72][73], see Fig. 4.12. The detn1 component is a result of derivative computation. The detn2 component is a result of division and sine approximation. The detn2 is calibrated with half bandwidth of the cavity. The final detuning is normalized using multiplication by the inverse value of 6.28 (1/2π).
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hardware computation result for 8 cavities is shown in Fig. 4.19. The latency for the most crucial components is summarized in Tab. 4.3.

![Graphs showing detuning for 8 cavities](image)

**Fig. 4.19. Detuning computation using FPGA implementation.** The input data for the hardware simulator was taken from monitoring ADCs of LLRF control of ACC 3 accelerating module. The vertical axis are in digital units of FPGA device.

**Tab. 4.3. The detuning computation summarize for single cavity.**

<table>
<thead>
<tr>
<th>Component</th>
<th>Latency [clocks]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cordic pipe</td>
<td>13</td>
</tr>
<tr>
<td>Divider pipe</td>
<td>4</td>
</tr>
<tr>
<td>Sine_pipe</td>
<td>3</td>
</tr>
<tr>
<td>Forwa_cal_pipe</td>
<td>3</td>
</tr>
<tr>
<td>Fir_pipe</td>
<td>6</td>
</tr>
<tr>
<td>Detn_pipe</td>
<td>3</td>
</tr>
<tr>
<td><strong>∑</strong></td>
<td><strong>32</strong></td>
</tr>
</tbody>
</table>

The algorithm latency for 8 cavities equals to 40 (32+8) clock cycles. The typical sampling frequency of LLRF control system is 1 MHz. For the system clock frequency of 100 MHz, the detuning algorithm takes less than 50 clocks which gives additional 50 clocks for control loop operation before the next sample. The full design of hardware simulator has been routed using ISE design software from Xilinx. The compilation report is shown in Fig. 4.20.
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4.4. DC Characteristics of Piezo Element

The DC characteristics of piezo element were measured to estimate the transfer functions demand for digital controller development. The open loop operation of the controller was applied for the experiment. The main idea was to measure the cavity detuning using the RF signals (plant response) and compensate it manually using fast frequency tuners (generate control input). The experiments were carried out for different accelerating field gradients increased by defined number of steps [72][73]. Since the main requirement for the piezo control is to compensate the Lorentz force detuning for high accelerating field gradients up to 30 MV/m, the ACC 6 accelerating module equipped with high gradient cavities was chosen for the experiment. The first series of tests were carried out using ACC 6 module installed in MTS. The MTS installation allowed for operating each cavity with its accelerating field gradients limitation (maximum operating conditions). The second series of tests were performed using ACC 6 module installed in FLASH facility. The FLASH installation allowed for operating each cavity with its nominal accelerating field gradients (nominal operation conditions).

For the MTS installation, the RF pulse duration as well as its repetition rate were set to 800 µs and 2 Hz, respectively. The 1st compensation scheme was used for all generated piezo compensation pulses. The accelerating field gradient for each cavity operation was adjusted from 20 MV/m up to 35 MV/m with single step of 5 MV/m (see Tab. 4.4). The

Fig. 4.20. The compilation report of designed hardware simulator using ISE design software from Xilinx.

The implemented hardware simulator has been further evaluated and used for development of the fast frequency tuners controller.
DC characteristics of piezo elements measured during the first series of tests are shown in Fig. 4.21.

For the FLASH installation, the RF pulse duration and its repetition rate were set to 300 µs and 5 Hz, respectively. The 2nd compensation scheme was applied to piezo pulse generation. The accelerating field gradient for each cavity operation was adjusted from 15
MV/m up to 30 MV/m with single step of 2 MV/m (see Tab. 4.4). The DC characteristics of piezo elements measured during the second series of tests are shown in Fig. 4.22.

Fig. 4.22. The DC characteristics of piezo elements used as actuators for ACC 6 (FLASH). The cavity 5 was not compensated due to known problem with mechanical installation of piezo tuner.
Tab. 4.4. Accelerating field gradient measurements for ACC 6 for MTS and FLASH installations.

<table>
<thead>
<tr>
<th>cavity no.</th>
<th>MTS accelerating field gradient [MV/m]</th>
<th>FLASH accelerating field gradient [MV/m]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>35</td>
<td>30</td>
</tr>
<tr>
<td>2</td>
<td>30</td>
<td>29</td>
</tr>
<tr>
<td>3</td>
<td>35</td>
<td>31</td>
</tr>
<tr>
<td>4</td>
<td>33</td>
<td>29</td>
</tr>
<tr>
<td>5</td>
<td>20</td>
<td>19</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
<td>21</td>
</tr>
<tr>
<td>7</td>
<td>30</td>
<td>24</td>
</tr>
<tr>
<td>8</td>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

The DC characteristics, measured for the maximum (cav1@35 MV/m for MTS) and for the nominal (cav3@)31 MV/m for FLASH) operating conditions of TESLA cavities, have been fitted with good result ($R^2>0.9$) using linear function (see Tab. 4.5). It is thus observed that the resulting slopes of linear fitting vary a little from cavity to cavity, their average values for all 8 cavities are of order of 5.7 Hz/V in the 1st compensation scheme and 3.6 Hz/V for the 2nd compensation scheme. The main difference between both estimated average slopes mainly comes from the fact that the different RF pulse durations have been set for both experiments.

Tab. 4.5. The resulting slopes derived using linear fitting of measured DC characteristics of piezo elements.

<table>
<thead>
<tr>
<th>cavity no.</th>
<th>MTS resulting slope [Hz/V]</th>
<th>FLASH resulting slope [Hz/V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5.4</td>
<td>2.7</td>
</tr>
<tr>
<td>2</td>
<td>5.0</td>
<td>3.4</td>
</tr>
<tr>
<td>3</td>
<td>7.6</td>
<td>3.6</td>
</tr>
<tr>
<td>4</td>
<td>5.9</td>
<td>4.8</td>
</tr>
<tr>
<td>5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>7</td>
<td>2.6</td>
</tr>
<tr>
<td>7</td>
<td>3.2</td>
<td>3.7</td>
</tr>
<tr>
<td>8</td>
<td>5.4</td>
<td>4.6</td>
</tr>
<tr>
<td>average</td>
<td>5.7</td>
<td>3.6</td>
</tr>
</tbody>
</table>

### 4.5. Control Algorithm

The measured DC characteristics have been used to develop the desired type of controller. As a proof of experiment, the Proportional gain controller (P) with the following transfer function has been chosen

$$V_{\text{piezo}} = K_p \cdot \Delta \omega$$  \hfill (4.35)
where $K_p$ and $\Delta \omega$ mean the inverse value of resulting slope coefficient and normalized cavity detuning, respectively [74][75]. The block diagram of control algorithm is shown in Fig. 4.23.

---

**Fig. 4.23.** The block diagram of control algorithm applied for the Lorentz force detuning compensation.

The control algorithm is activated by trigger signal. The trigger signal is used to start the cavity detuning computation for current RF field pulse. The RF pulse counter is applied to
store the flattop and decay detuning samples. The flattop detuning is calculated using the following formula:

\[
\Delta \omega_{ft} = \omega_1 - \omega_2 \tag{4.36}
\]

where \(\omega_1\) and \(\omega_2\) mean the flattop and decay detuning. The decision block is added to compare the flattop detuning with user defined limiter value. If the flattop detuning is higher than the limiter value the new correction for the piezo compensation pulse is computed. If the flattop detuning is lower than the limiter value, the algorithm waits for the next RF field pulse. The piezo compensation pulse correction is computed according to the formula

\[
amp_{corr}(k) = amp_{corr}(k - 1) + K_p \Delta \omega_{ft} \tag{4.37}
\]

where \(K_p\) means the proportional gain of the controller. The control algorithm assumes the fact that the cavity flattop detuning may be treated as linear function with positive, negative or zero slope with a different offset value (typically \(\pm 300\) Hz), as shown in Fig. 4.24. When \(\omega_1\) and \(\omega_2\) values of the detuning over the flattop are positive and the \(\omega_1 > \omega_2\) dependence is fulfilled, the piezo pulse correction is added to the one computed in the previous algorithm step. When \(\omega_1\) and \(\omega_2\) values are positive and \(\omega_1 < \omega_2\) dependence is fulfilled, the piezo pulse correction is subtracted from the one computed in the previous algorithm step. Since the control algorithm measures the cavity detuning from the current RF pulse and applies the correction to the next RF pulse, it will be then called the feedforward control.
4.6. The Application for Adaptive Feedforward Control

The practical application has been designed to test and validate proposed feedforward control. The application consists of digital control system with ADC inputs and DAC outputs, an 8-channel piezo driver unit and digital down-converter for sensing the RF signals (see Fig. 4.25). The digital control system is based on Simcon DSP prototype boards. A single board is capable of sensing and driving 8 input/output signals. The configuration of three boards connected with optical links allows for sensing 24 RF signals. The forward, reflected power and cavity voltage signals are used for computing simultaneously the cavity detuning for 8 cavities. The RF signals from the cavity are down-converted and sensed with desired sampling frequency using ADC converters. The DAC converters are used for driving the power amplifier with low voltage signals of ±1 V. The 8-channel piezo driver is used for driving the piezo actuators with voltage levels of the order of ±85 V.
The hardware platform, with control application, was installed temporarily in ACC6 of FLASH facility. The Simcon DSP boards (one master and two slaves) were installed in a VME crate while the 8-channel piezo drivers (with an integrated power supply unit) were installed in a Eurocrate. The compensation system was synchronized with RF pulse using a trigger signal of repetition rate of 5 Hz. The ADC channels of each Simcon DSP board were connected to monitoring ADCs of LLRF control system for reading the raw data of RF signals. The sampling frequency of the Simcon DSP ADCs was set to 1 MHz. The master board - controller was connected to an 8-channel piezo driver unit. The power amplifiers were connected to piezoelectric tuners operating as actuators. The Lorentz force detuning computation unit was calibrated for crosstalk attenuation between forward and reflected signals. The control tables were setup for each cavity with sinusoidal excitation using the full range of 18-bit 2’ complement representation. The time advance to RF pulse and the frequency of each piezo compensation pulse were set to 2 ms and 250 Hz, respectively. Finally, the proportional gain controller coefficients for each cavity were experimentally tuned. The compensation system was turned on and its efficiency was measured for different set points of cavity voltage (SP), as seen in Fig. 4.26, Fig. 4.27, Fig. 4.28, Fig. 4.29.
Fig. 4.26. The Lorentz force detuning measurements (cavity response) with piezo feedforward control (top) for SP 9.05 MV and forward power 190 kW (bottom).
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Fig. 4.27. The Lorentz force detuning measurements (cavity response) with piezo feedforward control (top) for SP 10.05 MV and forward power 217 kW (bottom).
Fig. 4.28. The Lorentz force detuning measurements (cavity response) with piezo feedforward control (top) for SP 11.05 MV and forward power 242 kW (bottom).
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Fig. 4.29. The Lorentz force detuning measurements (cavity response) with feedforward control (top) for SP 12.05 MV and forward power 264 kW (bottom).
To conclude, the applied control scheme was able to reduce significantly the Lorentz force detuning over the flattop region for all cavities over a single accelerating module. The cavity 5 was not compensated due to known problems with piezo tuner assembly and it was used as a reference value for uncompensated detuning. The compensated detuning has been kept constant for the full range of klystron operation from 190 kW up to 264 kW (measured per single cavity). The control output signal has been adapted automatically to different settings of cavity set point voltage and has not exceeded 40 V, as shown in Fig. 4.30.

The experiments that were carried out mainly proved that it is possible to reduce superconducting (SC) cavity detuning from electrical resonance frequency of 1.3 GHz to below 10 Hz for high accelerating field gradients operation of order of 30 MV/m. This fact proves the second thesis of this dissertation.

Even though, carefully designed hardware platforms allow for simultaneous Lorentz force detuning compensation of more than 8 cavities, the further development of the piezo control system was very much in demand. First of all, the usage of LLRF SimconDSP control board with 8 output driving channels was not so efficient for more than one accelerating module compensation. What is more, the piezo sensor readouts using LLRF control board were not so easy due to the lack of signal conditioning circuits. Since the cost of the single Simcon DSP board was twice as much as the price of the 8-channel piezo driver box, the design of the compact multichannel piezo control system was also initiated.
Fig. 4.30. The histograms of piezo voltage (controller response - top), Lorentz force detuning (cavity response - middle) and accelerating field gradient (operating conditions - bottom) for SP 9.05÷12.05 MV. The cavity 5 was put off from the closed loop operation due to a known problem with mechanical tuner assembly.
5. THE FAST FREQUENCY TUNERS CONTROL FOR FLASH

The control system for the fast frequency tuners developed with the use of Simcon DSP board is suitable for automatic and simultaneous compensation of 8 cavities. Since the FLASH facility is composed of 7 accelerating modules and 5 of them are equipped with fast frequency tuners, the several Simcon DSP boards should be used to meet such a configuration. The new design of multichannel digital driving and sensing circuit was used to reduce the number of control boards. The proposed multichannel platform is a prototype system and it is planned to be used to evaluate the hardware, firmware as well as software solutions for incoming XFEL experiment. To fulfilled such a requirements the designed control system should be installed permanently and its performance should be verified by commissioning during a real machine operation.

Especially, its effectiveness should be measured and analyzed with maximum operating conditions of the FEL machine. This paragraph introduces the design of 32-channel hardware platform with special emphasis on the FLASH configuration and integration with LLRF control architecture. The paragraph is finished with a short report on performance measurements of the piezo control system during high energy physics experiments carried out in DESY research center.

5.1. 32-channel Control System

The 32-channel piezo compensation system has been designed to meet the FLASH configuration. The compensation system consists of RF down-converters, monitoring ADCs, industrial SPARC CPU computer, LLRF control board (Simcon DSP), multichannel digital driving/sensing board (32-channel DAC/PZS), 8-channel piezo drivers (PZD) and LLRF timing board [75][76][77]. The system block diagram is shown in Fig. 5.1.
The RF down-converters as well as LLRF monitoring ADCs are located in Eurocrate and they are the integral parts of the RF field control system. The communication between monitoring ADCs and SPARC CPU computer is performed with the use of dedicated DOOCS servers via Ethernet interface [28]. The SPARC CPU computer together with LLRF control and timing boards are located inside the VME crate. The communication between the boards is performed via VME bus interface. The 32-channel DAC/PZS board together with 8-channel piezo drivers are located inside Eurocrate and connected with backplane. The Simcon DSP board is connected to 32-channel DAC/PZS board with optical link. The fiber optics was chosen in order to eliminate the impact of the cables length. It also makes the system radiation-robust. The 8-channel piezo drivers are connected to fast frequency tuners using coaxial cables and dedicated piezo patch panels.

The FLASH installation of piezo compensation system is shown in Fig. 5.2. The RF signals are sensed by down-converters and LLRF monitoring ADCs. The SPARC CPU computer is used for cavity detuning, control tables computation and data processing. The Simcon DSP board is used for sending and receiving the feedforward and feedback control tables, respectively. The 32-channel DAC/PZS board is used to control the driving and sensing circuits [78]. The 8-channel piezo drivers are used for amplifying the correction signal to proper voltage levels required for the fast frequency tuners control.
5.1.1. Hardware Overview

The Simcon DSP board is equipped with Virtex2 Pro FPGA device from Xilinx with fast built in serial links of RocketIO [79]. The maximum data throughput of the serial link is 3.125 Gb/s. The 32-ch DAC/PZS board is based on Spartan 2 FPGA device from Xilinx combined with external serializer/deserializer (SerDes) device TLK2501 from Texas Instrument. The maximum data throughput of the SerDes is 2.5 Gb/s. The driving circuit is equipped with 32 channel DAC converter with fast 50 MHz Serial Peripheral
Interface (SPI). The maximum sampling frequency of DAC converter is 400 kSPS. The sensing circuit is based on parallel SAR ADC converter combined with 32-channel multiplexer. The maximum sampling rate of analog to digital converter is 20 MSPS. The multiplexer device is connected to signal conditioning circuits based on instrumentation amplifiers from Analog Devices. The external SRAM memory is added to the system for storing the control tables used by driving circuit. The maximum memory access is 10 ns, so it can be efficiently used for processing fast data between control FPGA and fast serial link. The 32-channel DAC/PZS board is shown in Fig. 5.3.

![32-channel DAC/PZS board](image)

Fig. 5.3. The 32-channel DAC/PZS board picture. The driving circuit is provided using backplane connector. The sensing circuit is situated on the front panel using D-SUB connectors.

### 5.1.2. Firmware Layer

The controller is implemented using VHDL description language. The control tables are stored inside the internal memory block of Virtex 2 Pro FPGA. The FPGA communicates with SPARC CPU using VME bus communication library. The control data is divided into 32 pages, each page has depth of 256 words. The 32-bit long configuration
registers are preceded by the user defined signature and are sent to the LSB word first. The configuration data is used for controlling delay of the correction signal due to the external synchronization signal (trigger). The system clock frequency of the Virtex 2 Pro FPGA is set to 100 MHz while the reference clock frequency of RocketIO circuit is set to 106.25 MHz (reference frequency for fiber optic standard). The double clock FIFO buffers are used on the transmitter and receiver side of the RocketIO component in order to synchronized both clock domains. The same synchronization scheme is performed for the Spartan 2 FPGA and TLK2501 transceiver. The control tables used by Spartan 2 FPGA are stored inside the external SRAM memory. In order to avoid data collisions on the SRAM memory bus, the dedicated arbiter block is added. The data received from TLK2501 transceiver is stored temporarily inside FIFO buffer when the SRAM memory is accessed by DAC converter. When there is no access to the memory, the FIFO buffer is transparent. The digital to analog converter used for driving the power amplifiers is controlled by using a state machine with a dedicated address decoder (DAC control). The data read from piezo sensors is synchronized to the external trigger signal by user defined signature. The analog to digital converter with multiplexer circuit is controlled by (ADC control) state machine using a configuration word sent by user. The block diagram of the controller together with data frameworks are shown in Fig. 5.4.

Fig. 5.4. The block diagram of digital controller [77].

5.1.3. Software Layer

The control application was coded in C++ programming language. It consists of two main applications integrated into DOOCS control framework. The first application is used for detuning computation (middle layer server). It takes data from monitoring ADCs using shared memory access (see Fig. 5.1). The raw data from ADCs is demodulated to I
and Q components, then computed according to the Lorentz force detuning equation. The calibration of the coupler directivities is performed for cavity side of the coupler and it is used for forward and reflected power crosstalk elimination. The middle layer server was coded for 8 cavities support. The DOOCS servers can be copied as many times as defined in special server configuration file. The described feature was used for computing the Lorentz force detuning for 40 cavities of 5 accelerating modules equipped with double piezo tuners.

The second application is used for compensating pulse parameters computation (front-end server). The re-calculated new parameters of feedforward table as well as feedback table are sent/receive to/from the hardware using DMA transfers on the VME interface bus. The feedforward table is composed of sine-like waveform amplitude, frequency, number of pulses changed variably as well as time advance to the RF pulse. The custom table was added, for the user defined shapes of the compensation signal. The data transfers are synchronized with the RF pulse using interrupts generated by timing board. The piezo driving as well as the piezo sensing circuits are synchronized using the same timing events – the start of RF pulse for each accelerating module. Both circuits can be easily applied in advance to the start of RF pulse for more sophisticated control schemes. The block diagram of coded software layer is shown in Fig. 5.5.

![Block diagram of software layer of the piezo compensation system.](image)

**Fig. 5.5.** The block diagram of software layer of the piezo compensation system.

### 5.1.4. Client Application

The expert panel has been designed as a client application communicating with desired DOOCS server to provide easy access to control the piezo compensation system by
The designed system of multichannel piezo compensation has been installed permanently in the FLASH accelerator since August 2009. The system was used for supporting such experiments as high gradient, high current beam acceleration (9 mA tests) performed in DESY in September 2009. The main report and conclusion drawn from carried out tests is presented in section 5 of this thesis.

The FLASH facility is used for different experiments in high energy physics. The most important are the ones that improve the lasing process as well as machine operation under maximum operating ratings. The long-pulse (800 µs), high beam-loading (9 mA) experiments are typically used for improving machine operation. The main goal for such tests is to demonstrate beam energy stability, its main limitations or even a qualify possible control overheads. The next subsection briefly describes and summarizes the most
important experiments performed with piezo compensation system support. During the tests the major requirements for the piezo compensation system have been met and improved. Finally, the effectiveness of piezo compensation system has been measured and analyzed for all accessible accelerating modules equipped with piezo tuners [80].

5.2. Cavity Tuning and By-passing

As it was already mentioned, allowing for cavity tuning and by-passing in a wide range of ±1 kHz is one of the requirements for the piezo compensation. The range of tuning and detuning has been investigated, first using single pulse and then applying the resonance excitation to the piezo actuator. During the first series of tests, all 8 cavities of chosen accelerating module have been detuned by amount of 500 Hz using step motor tuners. After that, the piezo compensation system with single pulse has been applied to tune the cavities to the resonance operation. The tuning process is clearly visible on the cavity detuning curve but also on the phase signal of cavity voltage (see Fig. 5.7).

![Cavity Tuning Experiment](image)

Fig. 5.7. The cavity tuning experiment using single compensation pulse – with (green) and without (red) piezo compensation (cavity detuning – top; phase of cavity voltage - bottom).

During the second series of tests only one cavity has been investigated. The cavity detuning has been measured first without compensation, then the full range of cavity tuning and by-by-passing has been investigated (see Fig. 5.8). For that process, the resonance excitation of 4 pulses has been applied.
In case of driving fast frequency tuner with carefully defined signals, it is possible to shift the cavity resonance frequency from positive to negative values of about of ±1 kHz. It means the fast frequency tuner can be used for such process instead of step motor tuner, what can increase significantly the lifetime of slow frequency tuners. Moreover, during the machine operation the particular cavities can be switched on or off from the acceleration chain in the limited range of single kHz but several times faster than using slow tuners. The further development in tuning and by-passing is also planned using constant DC offset of the voltage applied to the piezo translator.

5.3. **High Current, High Gradient Beam Acceleration**

The most important experiment, performed in DESY in September 2009, was high gradient, high current beam acceleration (9 mA tests). The experiment was performed for
the long beam trains of order of 800 µs and with accelerating field gradients up to 30 MV/m. During the 9 mA tests, the control system for fast frequency tuners was switched on and used to compensate the Lorentz force detuning for all accessible cavities (only three of the accelerating modules have been equipped with piezo tuners, just prior to FLASH upgrade). The dedicated Data Acquisition (DAQ) subsystem has been applied for storing the history of all crucial machine parameters during the operation. The obtained results are shortly summarized below.

5.3.1. Lorentz Force Detuning

The cavity detuning has been used as the reference for all performed measurements. As proof of principle, the cavity resonance frequency shift of more than 300 Hz has been compensated to close to 1.3 GHz (corresponds to 0 Hz on the vertical axis) for all cavities of chosen accelerating module ACC3 (see Fig. 5.9). Since the slow frequency tuners were not used during the experiment (mainly due to the fact that they could change the other machine parameters and disturb the other experiments performed simultaneously), for some cavities the static detuning has been not compensated to the demand range of less than 10 Hz.
5.3.2. Cavity Voltage Signal Amplitude

The cavity voltage signal (probe) is the first parameter used for estimating the effectiveness of the piezo compensation system. It is clearly visible that the decrease in the Lorentz force detuning causes the increase in cavity voltage signal (see Fig. 5.10). It is mainly because of less power loses in the system. As a result, more power can be saved and delivered to the cavity. The cavity voltage increase means more effective beam acceleration as it is proportional to the accelerating field gradient of the cavity.
5.3.3. Forward Power Amplitude

The forward power is the second parameter used for estimating the effectiveness of the piezo compensation system. As one can notice, the decrease in the Lorentz force detuning causes decrease in forward power transmitted to the cavity (see Fig. 5.11). It is mainly caused by the fact that the RF field controller measures the cavity voltage signal and compares it to the demand set point parameter. The error signal is gained and added to the klystron driving signal according to the RF field control algorithm [60]. If the cavity is driven on resonance, it reflects less power. As a result, the smaller error signal is measured...
by the controller. The less error signal means less klystron drive from the RF field controller point of view.

![Graph showing cavity forward power](image)

**Fig. 5.11.** The cavity forward power measured without (red) and with (green) piezo compensation (top). The histogram of cavity forward power measurement for accelerating module ACC3 (bottom).

### 5.3.4. Reflected Power Amplitude

The reflected power is the third parameter used for estimating effectiveness of the piezo compensation system. It is clearly visible that decrease in the Lorentz force detuning causes decrease in the power reflected from the cavity (see Fig. 5.12). The reflected power decrease means less power loses in the system and as a result increase in the quality factor of the loaded cavity.
Development of Control System for Fast Frequency Tuners of Superconducting Resonant Cavities for FLASH and XFEL Experiments

Fig. 5.12. The reflected power measurement without (red) and with (green) piezo compensation (top). The histogram of reflected power measurement for accelerating module ACC3 (bottom).

The example results of each parameter measurements for ACC5 and ACC6 accelerating modules taken for more than 100 samples using DAQ subsystem are summarized briefly in Fig. 5.13 and Fig. 5.14.
Fig. 5.13. The probe, forward and reflected, cavity detuning, flattop detuning as well as static detuning measurements with (1st and 2nd row) and without (3rd and 4th row) piezo compensation for cav#1 of acceleration module ACC5.
5.3.5. Piezo Control System Effectiveness

The effectiveness of the piezo compensation system is measured using forward power, cavity power and reflected power, as seen in Tab. 5.1. The cavity power is the cavity voltage (commonly in MV) multiplied by beam current (commonly 9 mA). The values without any sign, collected in Tab. 5.1, are the absolute values measured without piezo compensation for the flattop duration of the RF field pulse (the time duration of
Since the cavity voltage signal is proportional to an accelerating field gradient inside cavity, the increasing of the power inside cavity means the improvement of the beam acceleration (see Fig. 5.15).

Tab. 5.1. Piezo compensation system effectiveness for 23 cavities of DESY FLASH.

<table>
<thead>
<tr>
<th>Cavity no.</th>
<th>Forward power [kW]</th>
<th>Cavity power [kW]</th>
<th>Reflected Power [kW]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Piezo off</td>
<td>Piezo on</td>
<td>Piezo off</td>
</tr>
<tr>
<td>1</td>
<td>116 -30</td>
<td>175 +15</td>
<td>25 -24</td>
</tr>
<tr>
<td>2</td>
<td>160 -17</td>
<td>178 +8</td>
<td>74 -66</td>
</tr>
<tr>
<td>3</td>
<td>148 -21</td>
<td>174 +6</td>
<td>56 -47</td>
</tr>
<tr>
<td>4</td>
<td>120 -23</td>
<td>170 +24</td>
<td>50 -46</td>
</tr>
<tr>
<td>5</td>
<td>118 -23</td>
<td>158 +30</td>
<td>70 -61</td>
</tr>
<tr>
<td>6</td>
<td>129 -23</td>
<td>173 +17</td>
<td>47 -44</td>
</tr>
<tr>
<td>7</td>
<td>136 -16</td>
<td>172 +17</td>
<td>54 -48</td>
</tr>
<tr>
<td>8</td>
<td>110 -15</td>
<td>164 +12</td>
<td>52 -45</td>
</tr>
<tr>
<td>Σ(ACC3)</td>
<td>866 -160</td>
<td>1363 +130</td>
<td>426 -382</td>
</tr>
<tr>
<td>1</td>
<td>85 -10</td>
<td>153 +15</td>
<td>21 -18</td>
</tr>
<tr>
<td>2</td>
<td>86 -9</td>
<td>151 +8</td>
<td>13 -10</td>
</tr>
<tr>
<td>3</td>
<td>90 -14</td>
<td>145 +13</td>
<td>27 -22</td>
</tr>
<tr>
<td>4</td>
<td>88 -15</td>
<td>144 +11</td>
<td>24 -22</td>
</tr>
<tr>
<td>5</td>
<td>84 -9</td>
<td>148 +9</td>
<td>21 -18</td>
</tr>
<tr>
<td>6</td>
<td>86 -12</td>
<td>135 +16</td>
<td>24 -21</td>
</tr>
<tr>
<td>7</td>
<td>90 -12</td>
<td>136 +15</td>
<td>27 -25</td>
</tr>
<tr>
<td>8</td>
<td>83 -10</td>
<td>138 +13</td>
<td>22 -21</td>
</tr>
<tr>
<td>Σ(ACC5)</td>
<td>691 -92</td>
<td>1149 +102</td>
<td>179 -158</td>
</tr>
<tr>
<td>1</td>
<td>268 -29</td>
<td>230 +31</td>
<td>78 -54</td>
</tr>
<tr>
<td>2</td>
<td>311 -47</td>
<td>209 +30</td>
<td>126 -104</td>
</tr>
<tr>
<td>3</td>
<td>274 -24</td>
<td>209 +35</td>
<td>105 -89</td>
</tr>
<tr>
<td>4</td>
<td>270 -23</td>
<td>241 +6</td>
<td>48 -29</td>
</tr>
<tr>
<td>5</td>
<td>- -</td>
<td>- -</td>
<td>- -</td>
</tr>
<tr>
<td>6</td>
<td>102 -10</td>
<td>126 +20</td>
<td>16 -14</td>
</tr>
<tr>
<td>7</td>
<td>155 -19</td>
<td>162 +20</td>
<td>28 -24</td>
</tr>
<tr>
<td>8</td>
<td>157 -14</td>
<td>163 +25</td>
<td>47 -42</td>
</tr>
<tr>
<td>Σ(ACC6)</td>
<td>1536 -164</td>
<td>1338 +170</td>
<td>448 -356</td>
</tr>
</tbody>
</table>
The effectiveness of the piezo compensation system has been measured for all three accelerating modules and compared to the total cavity voltage of the FLASH machine. The obtained results mainly show that the reduction in forward power of the order of 160 kW, means an increase in cavity power of 170 kW with significant reduction of reflected power of 350 kW (when measured from the start of the beam acceleration region, for a single accelerating module composed of high gradient cavities). The measurements performed mainly proved that it is possible to assess the effectiveness of the Lorentz force detuning compensation system using measurements of forward power (transmitted to the cavity), reflected power (reflected from the cavity) as well as cavity power (stored inside the cavity). This fact proves the third thesis of this dissertation.

![Graph of cavity voltage with and without piezo compensation](image1.png)

**Fig. 5.15.** The total cavity voltage amplitude measured without (left) and with piezo compensation (right). On the vertical axis there is a MV/m, on the horizontal axis there is time in µs.

![Graph of forward power, cavity power, and reflected power](image2.png)

**Fig. 5.16.** The simulation of effectiveness of the piezo compensation system for XFEL experiment. The values are represented as absolute numbers.
In addition, the absolute value of the reduced forward power is about the same value as the increased cavity power and two times lower than the reduced reflected power. Using this dependence, the effectiveness of the piezo compensation system can easily be forecast for the large scale machines such as XFEL. The simple simulation for XFEL machine composed of 100 accelerating modules is shown in Fig. 5.16.
6. ATCA FOR FAST FREQUENCY TUNERS CONTROL

Several generations of modular instrument standards have been used in very large scale accelerator machines as well as detector systems. The standards such as Nuclear Instrumentation Module (NIM), Computer Automated Measurement And Control (CAMAC) and FASTBUS have been used for high energy physics from the latest 60s and processed as open industry standards with IEEE and ANSI in U.S. and the IEC globally. Nowadays, most accelerator control systems are built on VME standard with some migrations to VME eXtensions for Instrumentation (VXI), which is more suitable for better shielding and additional timing and triggering features for high speed instruments. All the systems have similar very high pin count backplanes, first of all to handle parallel data transfers between the data collection and processing modules with the time multiplexed results sent upward through a single crate controller. Almost a decade ago, it was quickly realized that the multiplexed parallel bus architecture would become obsolete as the base technology for data communications moved ever more strongly toward high speed serial links, especially between devices within a module. Newly preferred architecture became conceptually a stand-alone functional module accepting input of single voltage power, analog and digital data inputs, and a timing signal, that transmits digitally processed results to a single high-speed serial link. In 2004, PICMG consortium started its new design and called it Advanced Telecommunications Computing Architecture, mainly because it was preliminary dedicated for industries of Telecom and Computing. Currently, different architectures for LLRF control are under studies at many labs. The LLRF control of the Free Electron Laser in Hamburg in DESY or Horizontal Test Stand (HTS) in Fermi National Lab (FNAL) are still based on VME standard [81]. The VXI standard seems to be very attractive solution for multichannel control. The receiver chases consisting of the Multichannel Field Controller cards (MFC) can accommodate up to 96 channels of the New Muon Lab (NML) facility. Since highly available techniques for electronics design techniques are becoming standard practice in industries of Telecommunications, the high energy physics labs rapidly started their investigations on ATCA and microTCA (µTCA).
architectures. Collaborators at KEK, FNAL and DESY are leading the ATCA based LLRF control studies [83]. The ATCA and Advanced Mezzanine Card (AMC) standards offer modular design, hot-swapping as well as redundancy. The single ATCA shelf can handle up to 36 superconducting cavities to control the drive to the klystron and maintain its output power amplitude and phase in stable relationship to the beam.

The piezo compensation system is an integral part of LLRF control system of the FLASH facility [80]. It is based on VME standard and it is capable of compensating simultaneously up to 64 cavities. Even the existing piezo control system is reliable and effective it has many disadvantages. The most serious disadvantage is a lack of redundancy circuits, especially for power supply unit which is the most important block. The hot-swapping function is also most wanted feature, especially when broken part needs to be exchanged without switching off the main power supply.

Since the single RF station for XFEL facility will consists of up to 32 cavities and almost 25 RF stations will be placed along the main linac, it is necessary to control up to 800 cavities equipped with 1600 piezo fixture tuners. In order to meet configuration of such large scale machine, the ATCA architecture with its modular design, hot-swapping, redundancy for the most crucial circuits as well as single relatively high voltage power bus is proposed.

### 6.1. ATCA Architecture Overview

The ATCA standard is accomplished with chassis (shelf) cluster concept that is air-cooled, redundant for all main functions (power supply, network, controller, hub switch as well as diagnostic control layer) and scalable to large or small clusters down to a very small payload module. Furthermore, the shelf is capable of hot-swapping at both large ATCA carrier blade and smaller Advanced Mezzanine Card (AMC) modules, see Fig. 6.1. The chase also includes a backplane for Rear Transition Module (RTM) with IO for ATCA carrier, and separate shelf options for the AMC card called µTCA.
The ATCA Carrier blade can be used as standalone, however, it can be extended easily by AMC modules directly connected to AMC bays. The full-size ATCA Carrier board is mainly fulfilled for backplane connections using RTM module. One can distinguish three main Zones used for such backplane, see Fig. 6.2. Zone 1 provides connection for redundant power supply bus which is -48 V. Zone 2 is capable of transmitting fast serial data using Dual Star Fabric or even Dual Network Switch Module. Typically, it is used for fast serial links using RocketIO, PCIe\textsuperscript{12} or GbEthernet interfaces. Zone 3 area can be user defined and it is typically used for various digital and analog fast interconnections via RTM module.

\textsuperscript{12} PCIe – Peripheral Component Interconnect Express
Fig. 6.2. ATCA carrier blade with Rear Transition Module connected on backplane [80].

The faceplate of the typical ATCA Carrier board is accomplished with alignment pins, floating fastener, ATCA leds with blue one for indicating the module activation and deactivation as well as handle with intelligent Hot Swap Switch. Moreover, the backplane side of the Carrier board is supported by alignment features and keying. The ATCA Carrier boards are placed in a shelf which is supervised by a Shelf Manager. The Shelf Manager communicates with all ATCA boards, Power Entry Modules, Fan Trays, or other modules through (IPMB-0) - the dual, redundant I²C-based bus, common for all ATCA boards. The Shelf Manager Controller communicates with Module Management Controllers (MMCs) on AMC modules and Rear Management Controllers (RMC) through another I²C-based IPMB-L – the local bus, which connects MMCs and RMCs with an Intelligent Platform Management Controller (IPMC) on the Carrier Board [82].

6.2. Prototype System Overview

The prototype piezo control system has been designed and fabricated to replace the existing VME-based control system with the one based on the ATCA architecture. The designed hardware and software have been capable of driving simultaneously of up to 32 cavities equipped with the fast frequency tuners. The control applications applied in the system have been fitted to the main framework of communication protocols and interfaces.
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Department of Microelectronics and Computer Science

foreseen for ATCA-based LLRF control system [85]. The control system is composed of MPC8568E PowerQUICC III processor board from Freescale, XC5VLX50 Virtex 5 FPGA board from Xilinx, an external card with 32-channel DAC and 8-channel power amplifiers (see Fig. 6.3).

![Prototype control system overview](image)

**Fig. 6.3.** The prototype control system overview. Starting from the left, the laboratory power supply unit, 8-channel piezo driver, 32-channel DAC board, PowerQUICC III processor with Virtex 5 FPGA board and monitoring scope [85].

The PowerQUICC III processor board communicates with the Virtex 5 FPGA board via a PCIe bus. The implementation and configuration of PCIe endpoint device is fully supported by the chosen FPGA chip. The universal communication interface for FPGA based projects - Integral Interface is used to provide flexible access to user-defined registers and memory blocks via PCIe endpoint device. The FPGA device controls external 32-channel DAC board using fast SPI interface with a serial clock frequency of order of 50 MHz. The DAC unit is dedicated to drive the 8-channel power amplifiers with low-voltage signals. The power amplifiers are capable of driving the piezoelectric actuators with signals in the range of ±80 V.

### 6.2.1. The Control Applications

The piezo control applications have been divided into two main parts. The high level applications are dedicated to cavity detuning computation as well as proper
compensation pulse generation. The low-level applications are used for raw data translation and 32-channel DAC board control, (see Fig. 6.4).

Fig. 6.4. The block diagram of prototype control system with high-level and low-level applications functionality description [85].

The client application is used for data visualization and setup of compensation pulse parameter of the piezo control system. It can be a C/C++ stand alone application running on the personal computer or a dedicated DOOCS server. Communication between client and server applications is performed by using high level application PCIe library that is responsible for such transmission aspects as data encapsulation, data format conversions or device address translations. An appropriate device driver was implemented to allow user mode programs to exchange information with the PCIe hardware sub-systems as well as for development of various control algorithms. For the piezo control system, the cavity detuning is computed using the LCR model of the cavity, analyzed in details in section 4.3. The cavity detuning algorithm uses the measurements of magnitude and phase of power applied to the cavity (forward signal) and the probe signal which is proportional to the electrical field inside the cavity [71]. The RF signals are measured using fast ADCs. For the laboratory tests, the ADC channels have been replaced with memory blocks - AREA_PROBE. The measured raw data is demodulated to I and Q parts of the complex signal. The digital signals are stored inside AREA_IQ memories for further data processing, see Fig. 6.5. The recording time of 2 ms corresponds to the FLASH RF pulse duration. After this period, the interrupt is requested by Root Complex via the PCIe endpoint and the interrupt module implemented inside the FPGA device. The proper
interrupt handler routine is provided by a Linux device driver to serve the interrupt. The typical repetition rate of RF pulses is 100 ms. Therefore the required time window for the detuning computation of 32 cavities and other control applications should not exceed 98 ms. The detuning computation algorithm uses I and Q tables of probe and forward signals with a depth of 2048 words. It gives around 262144 transfers to serve the detuning computation for the 32 cavities \(2 \cdot (I+Q) \cdot 32\) of control tables.

![Block Diagram of Control Unit](image)

Fig. 6.5. The block diagram of control unit implemented in Virtex 5 FPGA device. It is composed of control finite response machines as well as main communication interface between control unit and PCIe subsystem [85][86].

The 32-channel DAC control application consists of several registers, including 2 Finite State Machines (FSMs), an address decoder and an internal memory block (Fig. 6.5). The registers named as WORD_NS, WORD_FS and WORD_DLY are used for controlling driving pulse parameters control, which store a number of samples, sampling frequency and time advance to the input trigger signal. The state machine - FSM piezo control is applied for samples redistribution between corresponding DAC channels. Moreover, the module is used for synchronizing generated pulses with the start of RF field pulse. The internal memory block - called AREA_SAMPLES - is used for storing samples of reference driving pulse shape and its depth is 32 k of 14-bit words. Each output channel has memory space for 1 kilo words but it can be easily changed to different pulse width and sampling frequency. The state machine – FSM DAC control - is applied in the system for control of the external DAC device with SPI interface using a dedicated input/output. The Reset and Clear functions have been added by a set of registers, e. g. WORD_RST, WORD_CLR to allow the DAC device for initialization and fast shutdown of the driving signals. The Reset function is called as fast as possible after powering the system.
Reset function sets the internal DAC offset registers to the desired level of 0 V. The Clear function can be toggled by the operator during the normal system operation and it asserts zero voltage level to all accessible DAC device outputs. Using the Clear function the operator doesn’t need to cancel the driving signals generated by the controller. After switching on the system all the outputs are driven with the same signals as before the system off state.

6.2.2. Experimental Results

The prototype 32-channel piezo control system was installed temporarily in the FLASH facility. The system was connected to three 8-channel piezo driver units to be able to compensate 24 cavities equipped with piezo elements in the accelerating modules ACC 3, 5 and 6. A proper MatLab script was written to measure the detuning of all tested cavities using data from monitoring ADCs and DOOCS server. The FLASH accelerator modules ACC 2, 3 and ACC 4, 5, 6 were operated with gradients of 15.34 MV/m and 11.66 MV/m, respectively. The cavity detuning was first measured without compensation and then the compensation system was turned on. The piezo feedforward tables were tuned to proper amplitude and time advance to the RF field pulse to obtain the successful result on the Lorentz force detuning compensation. The dynamic detuning (over the flat top region - time window between 600 µs to 1400 µs of RF pulse duration) for all compensated cavities was decreased from about 300 Hz up to tens of Hz, as shown in Fig. 6.6. The slow tuners based on step motors were not used during the experiment. The static detuning (static offset of detuning curve with reference to zero Hz on the vertical axis) is clearly visible for all compensated cavities.

The demonstrated prototype system for the Lorentz force detuning compensation allows defining the main communication protocols as well interfaces for the future planned ATCA-based piezo compensation system. The concept design and the block diagram of the proposed hardware and software architectures are discussed briefly in the next section.
ATCA – based Piezo Control System Concept

The main parts of the piezo control system are driving and sensing circuits. The driving circuits are composed of power amplifiers used for generating high voltage signals applied to piezo actuator. The power amplifiers are driven with low voltage signals using DAC converters. The sensing circuits are comprised of instrumentation amplifiers for conditioning signal of piezo sensor. The closed loop operation of the piezo control is accomplished using ADC converters [87]. The piezo driving circuits were decided to be located on ATCA Carrier board. The number of 16 power amplifiers have been placed as 4x4 matrix located in the center, on the top side of the ATCA Carrier board. The high voltage output signals from power amplifiers are connected to the Zone 3 connector. The current limitation for each provided signal was doubled using differential pin pairs. The piezo sensing circuits were moved to RTM module as there was limited space on the main carrier board. The faceplate of the RTM module was fitted to handle output and input signals (up to 16 of each type). The high voltage output signals are driven to piezo actuators using hot pin of used connectors. The case of the connector is used for feedback...
signal from piezo actuator for voltage and current sense purpose. The same scheme was forced to differential input signals taken from the piezos operating as mechanical vibration sensors. The power supply unit for piezo driving circuits was integrated into ATCA carrier and it is located close to Zone 3 area. The input power supply voltage of -48 V is converted to bipolar ±85 V using four DC/DC converters connected in series [88]. Moreover, the power supply voltage of -48 V is also down to 12 V using a dedicated ATCA DC/DC converter and then provided for corresponding (Low-dropout) LDO regulators. The output voltage of each LDO is monitored and can be switched on and off by IPMC controller situated on the ATCA carrier blade. The FPGA device is responsible for real time computing as well as controlling the DAC and ADC converters. The FPGA device is supported by built-in fast serial links such as RocketIO and SGMII that are used for communication with the outside world. The RocketIO interface is connected to hardware cross-switch device for full mesh configuration. It allows piezo control board for connection to the slots from 5 to 8 (for 8 slots rack) and from 5 to 14 (for 14 slots rack) of ATCA shelf. The SGMII interface is used for communicating with external device which provides physical layer for GbEthernet interface. The GbEthernet#1 interface is connected to Zone 2 connector and it is treated as a redundant communication channel with other ATCA boards. The GbEthernet#2 interface is placed to the front panel and it is planned to be used for fast debugging purpose of the crucial components. The TCP/IP stack implementation for embedded systems is supported by Lightweight IP (lwIP) open source code. Xilinx Embedded Development Kit (EDK) provides lwIP software customized to run on Xilinx Embedded systems containing either a PowerPC or a MicroBlaze processor. The ATCA-based piezo compensation system can be directly put into the ATCA shelf of LLRF control system or it can operated as a standalone box connected to the main LLRF control system using optical link. The fact makes the board more universal, since it can be efficiently used for both standards ATCA as well as µTCA. The functionality of the IPMC is fulfilled by a dedicated microcontroller with 6 built-in I²C interface bus drivers. It allows for eliminating usage of I²C interface bus expanders. The IPMC is responsible for buffering of the incoming IPMI messages, processing them and, when necessary, for generating appropriate IPMI response messages, when necessary. Furthermore, the IPMC controls the whole process of Field Replaceable Unit (FRU) activation and deactivation, when the Carrier board is inserted into, or extracted from the chassis. The IPMC provides
also the Shelf Manager with the information concerning the whole board (FRV Repository) and all sensors (Sensor Data Records) [81].

What is more, the role of the IPMC is to control the most important modules such as power supply units and communicate with MMC placed on the Rear Transmission Module. When the RTM module is connected to or disconnected from the ATCA Carrier board, the MMC is sending a proper message to IPMC and the high voltage power supply is switched off or on. The block diagram of the proposed ATCA-based piezo control system is presented in Fig. 6.7.

To conclude, the design concept of the ATCA-based piezo compensation system has been accomplished by integrating driving, sensing, power supply and signal processing unit circuits into a single Carrier board. The system is planned to be manufactured, assembled, debugged and finally tested with real machine operation for the end of 2010 (see Appendix D.).
7. SUMMARY AND FUTURE PLANS

This dissertation covers the recent research and development (R&D) activities of control systems for the fast frequency tuners of TESLA cavities and predicts the implications foreseen for large scale machines such as the FLASH and the planned XFEL. In particular, the framework of the presented activities is the effort toward the:

1. R&D of the driving circuit,
2. R&D of the control algorithm,
3. R&D of the control system.

The main result of these activities is the permanent installation of the target piezo control system and its commissioning for 40 cavities divided into 5 accelerating modules at the DESY FLASH facility.

The author’s contribution was the study of possible designs of high-voltage, high-current power amplifiers, used for driving the fast frequency tuners, shows that several parameters of such a device needs to be considered. The most important parameter is the input and output power estimation. This arises from the fact that the estimation is the most crucial issue for both power supply and power amplifier unit design. Furthermore, the integrated overvoltage and overcurrent, as well as monitoring circuits, cannot be omitted, since the piezo tuners should be monitored and protected. The results of experiments, jointly performed by the author, proved the possibility for designing of an 8-channel piezo driver unit (with true bipolar output voltage and current (±100 V, 1.5 A) and significantly low crosstalk levels (>60 dB) between integrated driving circuits), that enables simultaneous compensation of single accelerating module composed of 8 superconducting cavities. The current installation of these devices for the FLASH facility covers 4 units packed into single crate of Eurocard standard with an integrated power supply unit.

Another topic which is elucidated in this dissertation is digital controller development. This mainly covers:

1. cavity detuning computation and its hardware implementation,
2. automatic control of fast frequency tuners for multi-cavity configuration.
The cavity detuning computation is the most important input to the fast frequency tuners controller, because it gives the information about the cavity response to the applied compensation. With the use of LLRF control systems that are commonly based on fast FPGA devices, the possibility of hardware implementation of detuning computation has been considered. The author worked especially on applying the serial pipelined computations. This work made it possible to define the computation core latency as well as its hardware resource usage according to the multi-cavity configuration of the controller. This hardware resource usage is such that the piezo controller integration with RF field controller can be considered.

The main difficulty in applying the hardware implementation of cavity detuning has been further exploited in the case of the automatic control of fast frequency tuners. The experimental analysis of DC characteristics of the piezo elements has shown the benefits of applying a small number of hardware resources for implementing of the control algorithm based on the proportional gain control scheme. As a proof of this principle, the experimental results from the first tests of the controller have been successfully performed and demonstrated for high-gradient operations of TESLA resonators.

The digital controller development would not be possible without dedicated digital hardware platforms. The 8-channel control system has been developed by the author of this thesis using Simcon DSP boards designed by LLRF control group. The experience gained in the field of the design and development of the digital control systems makes it possible to design a dedicated control board equipped with integrated 32-channel driving and sensing circuits. The designed hardware platform has been integrated with LLRF control systems and installed permanently at the FLASH facility.

Finally, the experience gained with control system commissioning during machine operation close to the maximum operating conditions has been reported. Preliminary tests performed during high-gradient, high-current experiment (9 mA) show that the installed system:

1. is capable of compensating of dynamic as well as static cavity detuning over the flattop region for less than 10 Hz,
2. is suitable for compensating simultaneously of up to 32 cavities,
3. can be operated efficiently with RF pulse repetition rates of up to 10 Hz,
4. allows for fast cavity tuning and by-passing in a demand range of ±1 kHz.
Measuring effectiveness of piezo compensation system has been one of the important issues studied during the machine operation. The RF control was measured first without piezo compensation and next with piezo compensation for a single accelerating module using forward power, cavity power as well as reflected power measurements. The obtained results show that RF control efforts for large scale facilities (such as the XFEL) can be reduced in the range of 10-20 MW. This is especially true for facilities containing one hundred accelerating modules. For single accelerating module equipped with high accelerating field gradient cavities, the reduced input power can be used efficiently for improving the beam acceleration especially when the module is last part of the FEL machine.

7.1. Future Plans

Even though the piezo compensation system has been developed and the main studies from its commissioning have been well understood, new paths of research are needed and predicted. First of all, the work on optimizing the piezo compensation pulse parameters has been postponed. The main aim of the research is to minimize the piezo compensation pulse efforts.

One of the important issues, that have been investigated briefly in Appendix B of this thesis, is the mechanical vibration attenuation using feedback information taken from piezo sensors. The proposed solution of using the second compensation pulse (fine tuning) has been analyzed. Basing on the analysis, it has been decided to use the second compensation pulse to support the high energy physics experiments that needs a very stable beam energy (SASE tuning) without any external disturbances, especially those coming from the piezo compensation pulse.

Finally, the reports on the tests for new, conceptually designed hardware platforms are very promising owing to the opportunities of new architectures such as ATCA or µTCA.
BIBLIOGRAPHY


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Appendix A: The Accelerating Field Gradient Vs. Pulse Amplitude

The cavity detuning has been measured and then compensated for the different accelerating field gradients. The optimum piezo pulse amplitude has been defined for each operating condition. The 2 MV/m step of accelerating field gradient has been decided to start from 16 MV/m for the nominal operating conditions. The 5 MV/m step has been decided to start from 20 MV/m for the maximum operation conditions. The results of measurements are collected in Tab. 7.1 and Tab. 7.2.

Tab. 7.1. The gradient vs. piezo pulse amplitude measurements for nominal operating conditions.

<table>
<thead>
<tr>
<th>Cavity no.</th>
<th>Gradient [MV/m]</th>
<th>Flattop detuning [Hz] piezo off</th>
<th>Flattop detuning [Hz] piezo on</th>
<th>Piezo amplitude [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>21</td>
<td>52</td>
<td>5</td>
<td>19</td>
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Tab. 7.2. The gradient vs. piezo pulse amplitude measurements for maximum operating conditions.

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<th>Flattop detuning [Hz] piezo on</th>
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Appendix B: Mechanical Vibrations

The piezo compensation signal can generate additional vibrations for the pulsed operated cavities with high repetition rates up to 10 Hz, (see Fig. 7.2). The induced mechanical vibrations can modulate the resonance frequency of the cavity for the next RF field pulse. Since, the RF linac can be operated with the short wavelength FEL radiation using SASE tuning, the effect can significantly disturb the experiment and do not allow for further machine operation with demand conditions (see Fig. 7.1).

Fig. 7.1. The beam energy monitor with piezo compensation (23:38÷23:40) and next without piezo compensation (23:40÷23:43).

The second compensation pulse has been applied in order to eliminate such a phenomena. Its main parameters have been discovered using piezo feedback information.
The experiment has been carried out in the following conditions. The Lorentz force detuning for chosen cavity has been measured and then compensated using properly tuned compensation pulse, as seen in Fig. 7.3. Next, the second piezo compensation pulse has been setup initially and applied after the current RF field pulse.

The optimum parameters of the second compensation pulse have been found using scan method according to the following steps:

1. fix the time shift after RF field pulse, scan amplitude,
2. find the minimum of the standard deviation of piezo sensor signal readout (region from 0÷150 samples),
3. fix the amplitude discovered from the found minimum, scan time shift after RF field pulse (see Fig. 7.4),
4. find the minimum of the standard deviation of piezo sensor readout,
5. repeat steps 1 to 4 with discovered parameters.

Fig. 7.4. The example feedforward (top) and feedback (bottom) for delay scan of the second compensation pulse [80].

After the optimum parameters investigations of the second compensation pulse were investigated, the mechanical vibrations have been measured first without and then with second compensation pulse. The obtained results for the last step of performed scan method are shown in Fig. 7.5. As it is observed, the standard deviation has been minimized from 0.015 up to 0.005 what corresponds to the dumping ratio of mechanical vibrations induced by the first piezo compensation pulse.

Fig. 7.5. The uncompensated mechanical vibrations caused by the Lorentz force detuning compensation method (left) and compensated mechanical vibration using second compensation pulse applied after the current RF field pulse (right). The vertical axis are in Volts, the horizontal axis are in samples. The sampling frequency is 5.7 kHz.

The performed experiment proved that the mechanical vibrations caused by the Lorentz force detuning compensation signal can be attenuated actively using the second compensation pulse with carefully tuned parameters (fine tuning). The proposed method is
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in development stage and it is planned to be automated and added to the fast frequency tuners control, i.e. for SASE tuning operation improvement.
Appendix C: Crosstalk Investigations

The TESLA accelerating module is composed of 8 superconducting 1.3 GHz resonant cavities. The superconducting cavities are equipped with the frequency tuners for Lorentz force detuning compensation. Since, the frequency tuners are equipped with double piezos, one can be used for actuating and the second one for sensing. The actuating and sensing capabilities of piezo tuners can be also used for damping ratio estimation along the module. The information on the damping ratio of cavities is very important from the driving circuit point of view (possible crosstalk between the cavities) and therefore it was measured for ACC6 crymodule equipped with double stack piezo tuners. The first cavity was chosen as aggressor while the other cavities inside the module where victims. The measurement setup block diagram is shown in Fig. 7.6.

Fig. 7.6. The block diagram of crosstalk measurement circuit along ACC6 accelerating module.

The spectrum analyzer was used for measuring the transfer function between the voltage applied to piezo actuator of cavity 1 (lock-in-amplifier) and voltage read from piezo sensor of cavity 2 to cavity 8. The transfer functions for each cavity are presented in Fig. 7.7. As reference, the sensor output of cavity 1 was measured first and then scaled by factor of 20 to be comparable to the other cavities response.
Fig. 7.7. Crosstalk along the ACC6 accelerating module. The piezo actuator of cavity 1 was driven with 5 V sinusoidal signal at frequency sweep from 10 Hz to 2 kHz.

It is clearly visible that resonance between 200 Hz and 250 Hz is also visible on the other cavities along the module, i.e. cavity 4 or cavity 6. The higher resonances such as 380 Hz even dominant for cavity 1 (used as reference) are not transferred to the other cavities. The damping of the chosen resonance of 250 Hz along the module is presented in Fig. 7.8.

Fig. 7.8. The damping of 250 Hz resonance along the accelerating module of ACC6.

It can be additionally noted that, the crosstalk level between the cavities can be neglected according to the measured damping ratio of 60 dB. Therefore, the crosstalk level between driving channels is the most important parameter of the driving circuit to be considered.
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When it is not possible to eliminate the phenomena, its level should be as low as possible or just comparable to the crosstalk level across the accelerating module.

**Crosstalk Between Driving Channels**

The crosstalk between driving channels is the most important parameter of the 8-channel piezo driver unit. The crosstalk measurements were performed in such a way that the chosen channel was an aggressor and it was driven with nominal operating conditions, while the other channels were victims and their output voltage signals were measured without generating any driving signal. All 8 channels of the amplifier were loaded with capacitance of several $\mu$F. The example results are shown in Tab. 7.3. It is visible that, the highest measured crosstalk level is close to 60 dB and it was observed when the channel nr 7 was an aggressor. It was further realized that the current path on the layout of the printed circuit board of such channel needed to be improved. Since, crosstalk level of the other channels was above 70 dB, the other channels were not debugged.

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Appendix D: Printed Circuit Board Layouts

The 32-channel DAC/PZS board consists of 4 layers. The internal layers are used for proper termination of differential signals of frequency of order of 2 GHz. The back plane connectors are dedicated to power supply lines (left) and DAC outputs (right) – lower side of the board. The piezo sensor signals with timing synchronization as well as optical module are provided using front panel connectors – top of the board (see Fig. 7.9 and Fig. 7.10).

The 8-channel piezo driver board consists of 2 layers. The back plane connectors are dedicated to power supply lines (left) and DAC inputs (right) – top of the board. The signal monitoring outputs and high voltage outputs to the piezo actuators are provided using front panel connectors – bottom side of the board (see Fig. 7.11 and Fig. 7.12).

The ATCA-based piezo compensation board consists of 10 layers. The front panel connectors are used for optical module as well as GbE interface – left side of the board. The backplane connectors are dedicated to power supply lines (ZONE1), fabric interfaces (ZONE2) and high voltage outputs to the piezo actuators and low voltage inputs from the piezo sensors (ZONE3) – right side of the board. The stack of 10 layers has been decided in order to provide more than 10 power supply lines as well as more than 50 differential signals of frequency of order of 2 GHz (see Fig. 7.13 and Fig. 7.14).

The RTM module for ATCA-based piezo compensation board consists of 4 layers. The backplane connectors are used for high voltage input signals to piezo actuators and low voltage output signals from piezo sensors (ZONE3) – left side of the board. The front panel connectors are used for high voltage output signals to piezo actuators and low voltage input signals from piezo sensors – right side of the board. The main power supply lines are provided using backplane connectors (ZONE3) (see Fig. 7.15).
Fig. 7.9. Top layer overview of 32-channel DAC/PZS board.

Fig. 7.10. Bottom layer overview of 32-channel DAC/PZS board.
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Fig. 7.11. Top layer of 8-channel piezo driver board.

Fig. 7.12. Bottom layer of 8-channel piezo driver board.
Fig. 7.13. Top layer of ATCA-based piezo compensation board.
Fig. 7.14. Bottom layer of ATCA-based piezo compensation board.
Fig. 7.15. Top layer (left) and bottom layer (right) of RTM module for ATCA-based piezo compensation system.