Recent Developments in Control Software for Optical Synchronization Applications at DESY

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Abstract—Proper operation of FELs such as the Free-Electron Laser in Hamburg (FLASH) and the European X-Ray Free-Electron Laser (XFEL), which is currently under construction in Hamburg at DESY, requires many specific subsystems to be synchronized with a precision exceeding 10 femtoseconds. Those components are often separated by several hundred meters at FLASH or even kilometers in case of the European XFEL. Such distances mean that it is extremely difficult to use only conventional RF signal distribution in coaxial cables for synchronization because of high losses and excessive phase drifts, while electromagnetic interference is also an issue. Therefore, a laser-based synchronization scheme can be employed in parallel. In this case, the synchronization signals are transmitted via length-stabilized optical fibers. Such an architecture is currently being used at FLASH and will also be the main means of synchronization at the European XFEL. The hardware for such a synchronization system consists of many optical elements such as commercial lasers and self-built free-space and fiber optic setups. However, a significant part of it is also the electronics responsible for control, diagnostics and signal processing as well as high-level servers and front-end software running on those devices. Currently, the VME standard is used throughout FLASH as the basis for the control system digital hardware. For the European XFEL, however, an architecture with a high level of reliability and availability is required as well as one with higher data acquisition and processing rates. Because of that, the Micro Telecommunications Computing Architecture (μTCA) has been chosen. It is a fairly new standard, provides significantly better performance and employs modern technological solutions making it more suitable for modern accelerator applications than the older VME architecture. The paper presents the latest improvements in the control software for the optical synchronization system based on the VME standard. Servers for phase-locking the lasers as well as controlling the fiber link stabilization units are described in detail. Plans for migration to the new infrastructure are also outlined.

Index Terms—Control, DESY, European XFEL, FLASH, optical synchronization system, systems, VME, μTCA.

I. INTRODUCTION

The sub-10 femtosecond requirements [1], [2] for the synchronization of elements at FLASH and XFEL demand all the elements of the system to work well on their own but also in cooperation with each other. In case of the optical synchronization system, this means the optical setups have to be well arranged, e.g., with monitoring capabilities and measures of automation, and provide reliable operation. For this, a well-designed software architecture is mandatory to monitor, control and automate them. The sub-10 fs stabilization is obtained using an optical cross-correlator setup. It is used both for laser locking [3] as well as fiber optic link stabilization. Higher precision is difficult to currently achieve because of various noise sources and limited readout electronics capabilities. A detailed description of those mechanisms is beyond the scope of this paper but is well documented in the reference materials.

The authors first introduce the importance of the optical synchronization system, and the software controlling it, in the context of the entire FLASH machine. Then, they briefly describe the basic block used in all the applications—a proportional-integral-derivative (PID) regulator implemented in a Digital Signal Processor (DSP) [4]. The DSP firmware communicates directly with the front-end Distributed Object-Oriented Control System (DOOCS) servers [5]. Also, the authors focus on the more advanced features of the middle-layer DOOCS phase-locking software for lasers and link stabilization units such as automatic switching between reference signals, error recovery routines, automatic signal discovery, and tuning. Exception handling procedures and future development plans are also described. The overall structure of DOOCS software layers is presented in Fig. 1.

The optical synchronization system is comprised of a Master Laser Oscillator (MLO), used as synchronization reference, and fiber links that transport the laser light to various endstations. The laser is phase-locked to the RF master oscillator in order to obtain unique timing throughout the accelerator. The stabilized fiber-links transport the signal to endstations, like the bunch arrival time monitors (BAM), different lasers such as the Pump-Probe (PP) laser [7] and, in the near future, also to the Low Level Radio Frequency (LLRF) system as a phase-stable reference signal.
The described optical scheme is important for accelerator subsystems, where high precision synchronization is needed (see Fig. 2). One of them is the longitudinal beam energy feedback (beam-based feedback, BBF), where the energy of the bunch is determined by the arrival time, taking advantage of the fact that electrons with different energies take different paths to travel in bunch compressors.

The ability to obtain high precision by fiber optic link stabilization at the 10 fs level makes it possible to reduce the bunch arrival time jitter below 50 fs [8], which significantly improves the efficiency of the FEL generation in the Self-Amplified Stimulated Emission (SASE) process. The arrival time of the traveling bunch is measured by the BAMs [9].

The BBF is closed through the LLRF system, which drives the accelerating RF field in the cavities. It does not replace the LLRF, but runs on top of it. A typical LLRF control scheme involves stabilizing the beam indirectly. It is focused on the stabilization of the amplitude and phase of the RF field in the cavities assuming that an increased field stability results in an increased beam stability. This additional feedback loop increases the efficiency of the LLRF control, because it is locked directly on the beam parameters. This significant improvement of machine operation would not be possible without the highly precise optical synchronization system.

The described systems interact also on the control software level. Some software components, such as control servers, exchange data with each other. For example, the BAM server may periodically check the state of the fiber optic link stabilization system, to avoid unsynchronized (random) operation. This shows that the control software for optical synchronization is required to run in a stable and correct way and is relied upon by other control components crucial for proper operation of the machine. In addition, the European XFEL will primarily depend on the optical synchronization system because larger distances between components make proper synchronization even more important.

II. VME-BASED HARDWARE PLATFORM FOR CONTROL PURPOSES

The control system hardware infrastructure of FLASH is currently based on the VME standard. A typical VME crate used for optical synchronization applications, as depicted in Fig. 3, consists of several boards: a CPU module implementing the server software; a storage blade; a timing card, which distributes trigger and clock signals to other boards; an analog-to-digital (ADC) card; a digital-to-analog (DAC) module and a digital signal processing (DSP) blade. The three latter boards form the basis for the feedback loop which is used wherever active control of system elements is required.

The ADC module consists of eight AD9240 analog-to-digital converters with a 14-bit resolution which can support a sampling rate of up to 10 Msamples/s. The analog characteristics, such as signal level range or input impedance, can be adjusted separately for each channel using on-board jumpers. The eight digital-to-analog converters on the DAC card are THS5671 chips. Their resolution is also 14 bits and they can provide voltages of up to ±6.3 V. However, in the DSP configuration discussed here, only two channels of the DAC module are available. The DSP chip is a Texas Instruments TMS320C6701 floating-point digital signal processor operating at 164 MHz. It is equipped with a Host Port Interface (HPI) which allows external hosts to access all the memory of the DSP over the VME bus. This feature is extremely important as it allows the higher-level DOOCS servers to easily read and write properties included in the firmware, such as regulator gains, and present them to the system operators. The ADC and DAC boards are clocked with a 1 MHz signal provided by the timing module, making it synchronized to other elements of the control system. The same module also provides a 10 Hz trigger signal synchronized to FLASH operation which is crucial when it comes to data acquisition timing and its processing.

III. CUSTOMIZABLE DSP-BASED PID REGULATOR

The core of the servers used for optical synchronization applications described here is the DSP firmware implementing a customizable proportional-integral-derivative (PID) regulator. Since the ADC board provides eight inputs and the DAC board is able to drive two outputs, the DSP firmware is designed in
such a way that two independent devices can be controlled by one DSP board. This allows each device to take advantage of up to four inputs and one output. For example, two different lasers, each with four different reference signals, can be phase-locked this way. In addition, each of the signal paths for each of the reference signals can have different values of the P, I, and D gains as well as the set-point (SP) and the cut-off frequency for a low pass infinite impulse response filter (IIRF), also implemented in the DSP firmware. This structure is presented in Fig. 4. The MUX in the figure represents the selection of the signal source and the parameters for each of the reference signals while the CTRL module includes the filtering stage and the PID regulator.

The customization and re-implementation of the PID algorithm in the DSP increased the bandwidth of the system which previously was less than 100 kHz. The results for various settings of the regulation loop are presented in Table I. These improvements resulted in one very significant optical synchronization system achievement. Using the previous implementation, the DSP was not able to control the cross-correlator based laser-to-laser synchronization which only proved possible with the higher bandwidth.

However, the speed and performance improvements are not the only features of the synchronization software. The ability to automate processes, handle exceptions and change various parameters without stopping the system are also important. Examples of such functionality are presented below where the middle-layer servers are described.

IV. MIDDLE-LAYER SERVER FOR LASER PHASE-LOCKING

This server is used to synchronize a laser’s repetition rate to a reference signal coming either from an RF source such as the RF Master Oscillator (MO) or another laser such as the MLO. In both cases, the controlled and the reference signals are converted to RF signals with a large bandwidth photodiode (PD) and sent to a phase detector [7]. Its output is then fed into the PID regulator which, ultimately, drives a piezo element which changes the length of the laser cavity, adjusting its repetition rate (see Fig. 5). This fairly standard way of phase-locking the lasers [10] is enhanced in the current implementation of the server by additional functionality. First, it has to be mentioned that in most of the setups more than one reference signal is used. There is one at the fundamental repetition rate of the laser and one or more at higher harmonic frequencies, depending on what signals are available. A common frequency is 1.3 GHz available from the MO, although 9.1 GHz is also used, for example in case of the laser system used for pump-probe experiments. The fundamental frequency is required to ensure a unique phase-lock relation between the laser and the accelerator while the higher harmonics help to achieve a tighter lock since the sensitivity of the phase detectors is greater.

The server allows the reference signals used in the control loop to be manually selected, providing moreover even two sets of PID gains for each of the inputs. This can be used by the operators depending on the outcome they desire. For example, a more relaxed gain settings can be used for locking the laser initially and then a more strict set of parameters can be selected to optimize the lock. Furthermore, an automatic switching procedure can be initiated, where the operator defines the sequence in which the laser is phase-locked to specific reference signals (from the fundamental frequency to the higher harmonics) and, upon successfully locking to one of them, moves to the next one. The server also provides monitoring and automatic control of the piezo driver voltage, making sure that it is always kept within a defined range. This functionality is described in more detail below. The operator panel for the MLO, designed using the jddd environment [11], is presented in Fig. 6.

TABLE I

<table>
<thead>
<tr>
<th># ADCs</th>
<th>IRF ON</th>
<th>Bandwidth [kHz]</th>
<th>ADC samples missed</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>YES</td>
<td>143</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>YES</td>
<td>166</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>NO</td>
<td>250</td>
<td>3</td>
</tr>
</tbody>
</table>

Fig. 4. Logical structure of the DSP-based double PID regulator.

Fig. 5. Laser phase-locking principle of operation.
A. Calibration and Automatic Coarse Tuning

Before any phase-locking of the lasers can take place, the particular setup needs to be calibrated in order to properly calculate the timing jitter of the phase-locked laser. This is done by measuring the sensitivity of the phase detector by observing the beat frequency it produces when the repetition rates of the target laser and reference signal are not equal. By calculating this frequency, as well as taking an average of the captured slopes of the signal, taking into account the sampling frequency of the DSP, it is possible to obtain a calibration coefficient ($K_{\theta}$) expressed in mV/deg of the mixing frequency. When this coefficient is known, all the signal variations in the voltage domain observed when the laser is phase-locked can be translated into the time domain giving a measure of the quality of the lock using the formula for timing jitter (1).

$$T_{\text{RMS}} = \frac{\varepsilon \tau_{\text{RMS}} f_{\text{mix}} \times 360}{K_{\theta}}$$  \hspace{1cm} (1)

This allows the operator to fine-tune the parameters of the regulation in order to improve the quality and thus lowering the timing jitter.

The DAC output voltage, ±6.3 V, is too low to drive the piezo element inside the laser cavity in the desired range. An additional piezo driver is required which will convert it to an acceptable level, that is 0 to 100 V in case of laser systems. Still, such a piezo range can only compensate a few kilohertz of drift of the controlled laser’s repetition rate. This means that it is possible to lose the phase-lock if the phase difference between the target laser and the reference signal drifts beyond this limit. A slow coarse tuning with a much larger range but a smaller accuracy is required in this case. There are currently two coarse repetition rate tuning schemes applied to the lasers used at FLASH that are phase-locked using the software described. One is based on temperature control and the other one uses stepper motors. The former tuning is employed in the commercial SESAM-based Origami laser, serving as MLO, where the SP of the internal temperature stabilization scheme can be modified [12]. In the latter case, one of the laser’s cavity mirrors is additionally mounted on a motorized translation stage. Both tuning methods can be set to execute automatically as soon as customizable thresholds for piezo voltage are crossed. In most of the cases a reasonable range of the piezo voltage is around half of the total range. For the MLO it is set between 15 V and 75 V. The tuning scheme choice does not require any changes for the SP of the internal temperature stabilization scheme can be modified [12]. In the latter case, one of the laser’s cavity mirrors is additionally mounted on a motorized translation stage. Both tuning methods can be set to execute automatically as soon as customizable thresholds for piezo voltage are crossed. In most of the cases a reasonable range of the piezo voltage is around half of the total range. For the MLO it is set between 15 V and 75 V. The tuning scheme choice does not require any changes for the SP of the internal temperature stabilization scheme can be modified [12].

B. Two-Piezo Tuning Setup

A slightly different type of tuning is employed in a Vectron oscillator used for the pump-probe experiments [13]. Two coarse tuning stages are available there. Between the small-range, fast piezo driven by the PID regulation and the long-range motor tuning, a second, slower piezo is installed. The first piezo can compensate for timing drifts in the range of around 25 fs while the second one extends the range that can be covered without driving the motor by another 150 fs. The second piezo voltage is held at a constant level until the first one crosses defined thresholds. Then, the voltage level is changed accordingly with a customizable step size. This step can be calculated in a way that the first piezo voltage drops right into the middle of its range making the necessary tuning actions as limited in number as possible. Also, when the larger-ranged piezo crosses its threshold and the motor eventually needs to be moved, the voltage level is modified to again keep the regulation piezo as close to the range center as possible. This kind of two-piezo tuning had not been possible with the old DSP firmware since it uses the two independent DAC outputs made available in the new implementation.

C. Automatic Reference Signal Switching

In order to minimize the timing jitter of the laser, phase-locking to higher frequency reference signals is performed. As a tradeoff for better short-term performance, the lock is getting less stable with greater frequencies. To make sure that the best possible lock for particular conditions is found, an automatic reference signal switching mechanism has been proposed and implemented in the server. The operator sets the mixing frequencies for all the inputs, which are defined by the phase detector hardware that is actually installed, in ascending order and then uses the functionality to calculate the calibration coefficients ($K_{\phi}$, see Section IV.A) for each of the mixers. The next step is setting the timing jitter thresholds for which switching is done. In the presented example, taken from the pump-probe laser, when the 108 MHz lock produces timing jitter of less than 1000 fs, switching takes place and the 1.3 GHz reference is used starting from the next ADC sample. Dropping below 20 fs causes the server to switch to a yet higher frequency phase detector operated at 9.1 GHz. As there are no higher frequency reference signals available the next threshold is set to −1 fs, which obviously cannot be crossed. If the lock deteriorates and the timing jitter gets higher than the reset threshold the whole procedure starts over from the lowest mixing frequency to ensure re-lock at the correct phase-relation with the accelerator (see introduction to Section IV). The reset can also be triggered manually or when the global threshold is exceeded.
Locking to a low frequency reference signal adjusts the repetition rate of the server in a good-enough way that a signal with no beat frequency at the higher frequency phase detector output appears. However, a phase mismatch may be observed at the ADC input, e.g., because of different cable lengths. This can be seen in the figures below, where the laser is locked to 108 MHz (ADC0, Fig. 7(a)) but the output of the 1.3 GHz phase detector is not zero (ADC1, Fig. 7(b)), indicating a phase difference between this reference and the controlled signal.

When switching, it is important to make sure that the DAC output, and in turn the piezoe voltage, changes as smoothly as possible. If the higher frequency reference PID is allowed to take over the control with an error signal proportional to the phase difference and a SP of zero, a point of significant discontinuity can be introduced. In order to avoid such jumps, a mean value of the ADC reading is calculated, which corresponds to the DC offset of the phase detector output, and introduced as the new SP of the target PID regulator (Fig. 8(c)). The previous SP level is stored. Also, the integrator value at the moment of switching from the lower frequency reference is kept. If both these conditions are met, the switching instant will not introduce large jumps in the DAC output [14]. Afterwards, the SP of the current PID regulation is restored in incremental steps (Fig. 8(d)), smoothly transitioning to the desired phase difference level, which is usually zero. The time needed for this operation depends on how far away the original SP is and on the update rate of the server. In the current implementation it takes up to a couple of seconds to restore the SP. The time is not that crucial in this case as the automatic switching procedure is usually carried out only once during initialization of the setup.

V. MIDDLE-LAYER SERVER FOR PHASE-LOCKING THE FIBER LINK STABILIZATION UNITS

The fiber link stabilization units are used for distribution of laser pulses of the MLO to remote locations along the accelerator tunnel with a particular precision. Their purpose is to minimize the timing drift of the pulses at the link end, aided by the control software. Relative timing changes can be measured using a balanced optical cross-correlator (OXC) installed inside the stabilization unit. The full optical setup of the OXC is out of scope of this paper, and can be found elsewhere [15], but the principle of operation will be presented here. The laser pulse train from the reference source (MLO) is split up into two parts. One of them is directly sent to the OXC arm and the other one is transmitted down the link. At the end of the fiber a small fraction of the light is reflected with a 90 deg rotation of linear polarization and returns to the OXC arm. The cross-correlation of the reference and reflected pulse trains takes place in a periodically-poled potassium titanyl phosphate (PPKTP) crystal, which requires perpendicular polarization states for the second-harmonic generation (SHG) process and occurs when pulses overlap temporally. The signal generated by the SHG process in the PPKTP is transmitted into the first detector of the balanced receiver. The second SHG process is required to find the timing relation between the pulse trains in a balanced, i.e., amplitude-independent, scheme. Therefore, the fundamental pulses are reflected and pass the PPKTP crystal the second time. Due to a different group velocity for light with perpendicular states of polarization, a delay is introduced between the fundamental pulses, which results in a small temporal shift of both generated second-harmonic signals. Because of this, the balanced receiver produces a bipolar signal with a steep slope around the zero-crossing. This, in turn, provides a very precise measurement for the relative timing of the fundamental pulses as the SHG process, and hence the produced output voltage of the detector, is very sensitive to the overlap of the pulses in the crystal. The floor level can be observed when pulses do not overlap. The valid timing information is available only when the OXC is set in the dynamic region, near the zero-crossing where the sensitivity is highest. The OXC characteristic can be seen in the lower left graph of the operator panel in Fig. 9.

A. Link Commissioning and Fast and Slow Control

The control algorithm implemented in the software needs to compensate for link length changes introduced by temperature drifts and mechanical stresses, e.g., introduced by vacuum pumps inside the accelerator tunnel, to keep the OXC in the dynamic range and provide valid information about link timing. A PID controller, similar to that used for laser phase-locking, has
been employed for this purpose. Its input is the OXC signal and it drives a fast piezo-based fiber stretcher installed in the link stabilization unit to compensate for the detected length change in the range of 15 ps. The fiber stretcher is used to fine tune the link. However, the drifts of the links exceed this value over longer time periods, so an additional motorized delay stage has been introduced into the laser pulse path. The motor is controlled by another software module which not only provides slow tuning of the link length, but also several new features not available previously.

The first one is automatic OXC signal finding routine. When a new link is set up or readjusted after a longer shutdown, the dynamic range of OXC has to be found. This procedure was done manually by connecting the OXC signal to an oscilloscope in the laboratory and driving the motor delay stage in order to find the correct position.

The new server is able to follow this routine automatically with a single click of a button. First, the OXC floor level is determined by moving the motor by large steps and reading the OXC signal value. Then, the motor is moved to a position where the OXC signal had been present the last time the link had been locked. If the last position is unknown the motor is driven to the middle of the available range. The software drives the motor with steps significantly smaller than the OXC pulse width, scanning for the OXC signal. If the signal is not found in proximity of the initial position, the program exceeds the range and repeats the procedure. If the link is in shutdown for a short time the signal is found very fast. In case of first scanning after setting up a new link or a long shutdown period, the routine can take up to 30 minutes. This limitation comes mainly from the communication delay between the server and an industrial controller driving the motor. Nevertheless, this procedure provides an automatic way of finding the OXC dynamic region without having to physically access the hardware.

B. Piezo Calibration

Another feature introduced into the server is determining the coefficient translating changes of the PID output (piezo voltage) to changes of link timing. The idea is to scan the whole DAC range, from −6.3 V to 6.3 V, by driving the delay stage motor. If the regulation loop stays closed and the motor is moving, the delay introduced by the motor is immediately compensated for by changing the piezo voltage. The number of steps made by the motor during scanning can be easily recalculated into distance, which then can be expressed as time. It allows to determine what timing change at the end of the link is introduced by a specific voltage change on the DAC output. In case of the test setup used during software development for one of the links available at DESY, the value of this coefficient was calculated at $K_{\text{piezo2ps}} = 1.24$ ps/V. This value is used during coarse tuning and for the fast calibration routine which are the next two features described below.

C. OXC Calibration

In order to find the OXC calibration coefficient ($K_{\text{OXC}}$), the slope of the OXC dynamic range needs to be found. Previously, this was done using a Matlab script by scanning the motor delay stage near the zero-crossing point which had to be found manually. Then, the received data was linearly approximated and the coefficient was determined. The same algorithm was transferred into the server. The main disadvantage of this approach is a very long time of execution because of the communication delay between the server and an industrial controller driving the motor. Therefore, drifts and other instabilities have significant influence on the received result. Moreover, scanning can only be done when the link is not in use, because the PID lock is opened and the link is not stabilized while the motor is moving. Furthermore, the absolute timing at the link end changes, which causes, for example, the overlap with the electron bunch in a BAM to be lost or the timing relation of a synchronized laser to be changed. Therefore, a new approach for fast calibration has been proposed and implemented.

Fast calibration is performed by the DSP firmware running the PID regulation, but is triggered from the middle-layer server. A sinusoidal excitation of controllable amplitude is superimposed on the last DAC output as shown in the top left graph in Fig. 10.

The excitation response is the OXC characteristic near the zero-crossing point (see bottom left graph in Fig. 10) which allows the $K_{\text{OXC}}$ to be calculated. The $K_{\text{piezo2ps}}$ coefficient is required here in order to translate the piezo voltage to time units. After the fast calibration, the PID resumes its usual operation. The biggest advantage of this approach is the amount of time it takes to do the whole calibration. In the current implementation, the sinusoidal excitation consists of 2048 points and the DSP processing rate is 200 kHz, which leads to 10.24 ms. For such a short period of time, link drifts are too small to have a noticeable impact on the obtained data. Therefore, the received values are constant and do not fluctuate between measurements as was the case with the slow calibration. Moreover, the fast calibration can be done periodically, even during machine operation, between the electron macropulses at a 10 Hz rate. Therefore, the timing relation of the reference pulse train and the end-stations in presence of the electron bunches is not disturbed by the calibration routine.

D. Automatic Coarse Tuning

The automatic coarse tuning of the link timing is in principle the same as in the laser phase-locking scheme. The delay stage
motor needs to be driven in order to compensate for the timing drifts that are beyond the range of the piezo-stretcher. What is different are three versions of the correction algorithm. In the simplest one the routine is finished just after the piezo-driver falls back within the limits set by the operator, which triggered the motor movement in the first place. The more advanced correction routine introduces hysteresis into the calculation. The piezo voltage limits are shrinked by the hysteresis factor \( H_f \) which may vary from 0 to 0.9. In this case, the end of correction happens when the piezo is in the range calculated by the formula \( (1 - H_f) \times V_{\text{limit, min}} < V_{\text{piezo}} < (1 - H_f) \times V_{\text{limit, max}} \). Here, the motor is also moved by a constant number of steps defined by the operator. The most advanced algorithm employs the \( K_{\text{piezo2 piezo}} \) coefficient. It allows the software to calculate the exact number of steps which the motor needs to be moved, in order to put the piezo voltage back into the desired limits. This makes the correction algorithm much faster because the bottleneck in the system is the communication between the server and the motor. In this case the server only has to generate a single command for the delay stage motor which significantly decreases the time of the correction routine. Not only is this type of coarse tuning the fastest one, it also limits the number of times the motor needs to be moved, extending its lifetime.

VI. Exception Handling

Other systems rely on the successful supervision of the devices by the servers described here for operation within their limits. Additionally, the hardware that is controlled has physical limits which should not be exceeded because of possible damage. This mostly applies to the stepper motors and piezo elements. In cases when those requirements are not met, appropriate actions need to be taken to make sure that no harm will be done to the rest of the machine as well as to inform the operators of possible problems so that it is easy to identify and solve them. This means that the exceptions need to be handled in software as far as control of the devices is concerned as well as in the operator panels where easy-to-read indicators and warning messages should appear. The latter action is very important since not all exceptions can be handled by software and expert intervention is necessary, for example when a laser loses its mode-lock.

In the setups discussed here there are two major common sources of exceptions that need to be handled by both servers.

A. Error Connecting to Hardware

In order to monitor and control properties such as the piezo voltage or the motor position, the software needs to connect to low-level servers or industrial controllers, that are responsible for communication with the hardware. An example of such a piece of software is the DSP server interacting with the PID regulator on the DSP chip. If those front-end servers fail, be it because of hardware communication issues or simply because they are stopped manually, the middle-layer servers do not have a way to obtain data such as ADC readouts or DAC output values. It is then impossible to determine the value of the piezo voltage the DSP regulator provides and so the control of this voltage may not take place. Similarly, the inability to connect to the motor driving server makes the coarse tuning unavailable. In both cases the coarse tuning functionality is disabled by the server and an indicator in the panel tells the operator that the status of the front-end servers is invalid.

B. Coarse Tuning Failure

It is also possible that the coarse tuning feature malfunctions and the piezo voltage level will not be brought back within the desired limits. This is a very unlikely situation but may happen if the motor is unresponsive, if some connections along the way fail, a fuse is broken or even if the piezo voltage jumps by a significant amount that is beyond recovery. In order to prevent driving the motor indefinitely, or temperature-tuning of the Origami laser, which can be even more harmful, only three tuning attempts take place. If those attempts do not cause the piezo voltage to come back into the threshold limits, the PID feedback loop is opened and the automatic tuning is disabled. This means that the phase-lock is lost, which is indicated in the operator panel, but usually in those cases the lock is already not there or is in a very unstable condition so it is safe to disable the regulation. An alternative, where the control loop acts on undefined signals driving the piezo in an unspecified way is unacceptable and thus avoided.

VII. Future Development of the Optical Synchronization Software

Although a lot of progress has been done over the last year, the optical synchronization software development faces new challenges and room for new functionality remains still. Also, the emergence of the \( \mu \)TCA standard [16]-[18] as the replacement of VME, especially in physics applications [19], [20], means that adaptation of the front-end software to the new platform needs to take place.

A. Migration to \( \mu \)TCA Infrastructure

The VME architecture is quickly becoming obsolete as the speed of the computation blades as well as the reliability and availability of the crates and modules becomes less satisfactory to be used in advanced control environments. Migration of the existing control system to run on a modern \( \mu \)TCA infrastructure is the next big challenge to be faced by the optical synchronization system. Some parts of the existing control systems at FLASH, for example the LLRF system, have already migrated to the new architecture with success during test runs [21]. The middle-layer servers described here are platform-independent and can run on any hardware structure that supports DOOCS. On the other hand, the low-level servers as well as the entirety of firmware of reprogrammable devices (FPGAs, DSPs, etc.) will be rewritten and redesigned to fully use the advantages of modern, fast hardware.

B. Laser-to-Laser Phase-Locking Control

It has been proposed to use the cross-correlator to lock a laser to a reference light source. This is similar to the approach used in the link phase-locking scheme, where the same light source is used as both inputs—one in the forward direction and the other one reflected from the link end. The details of the optical setup are beyond the scope of this paper but can be found in other publications [6]. In case of two light sources, the signal is less stable and the optical alignment is more difficult. Consequently,
the regulation gains need to be tuned with more care. Also, the switching between the phase detector reference signal and the OXC reference signal is more complicated because of the temporal characteristic of the latter signal. More accuracy in the switching procedure parameters is required. This feature is currently under development and first tests under laboratory conditions have been successful, taking advantage of the improved DSP-based regulation.

VIII. CONCLUSION

Last year resulted in a significant improvement of the software in control of the optical synchronization system at DESY. Several outdated servers got replaced with newer versions and many features have been added. This paper focused on two examples of the improved servers, both based on the redesigned, customizable, DSP-based PID regulator. The DSP firmware works now with a processing rate of up to 250 kHz which is an improvement of factor three compared to the previous implementation [4].

Most of the additions to the laser locking software and the link locking software were implemented to make those procedures less prone to human errors by automating activities previously done manually. Actions such as signal discovery for link locking or switching between different reference signals for laser locking are done with a single click, thus avoiding what earlier had to be done manually with an oscilloscope in the laboratory. This is especially important for devices that are placed in locations where access is forbidden or at least undesirable. For example, the MLO and the link boxes located in the synchronization hutch are highly sensitive to vibrations and temperature changes, which are obviously introduced with people walking around them. Now, with the automated procedures, in many cases, there is no need to physically be present near the equipment. Furthermore, with the redesigned operator panels, it is much easier to recognize possible errors in the system due to indicators that are driven by exception handling routines implemented in the software. The presented middle-layer software solutions are hardware-independent and the code is portable to any architecture able to support DOOCS used at DESY. Therefore tests of the software can be thoroughly performed at FLASH and later seamlessly moved to operate in the European XFEL environment.

The next big step for the optical synchronization system is the migration to a modern μTCA infrastructure. However, the middle layer servers are architecture-independent and will be able to work on top of the new firmware and front-end software which are also under development. A step up in the computational power capabilities as well as data transfer and acquisition speeds will result in an increased performance of the optical synchronization system in terms of maximizing stability of crucial components such as fiber link units and MLOs. With the increased performance the stability of the cross-correlator based synchronization schemes will also be improved.

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REFERENCES